R63 INTEL SYSTEM DIAGRAM

01

+3V/+5V S5 PG.36
+1.05V PG.37
CPU Core PG.40~41
DDR3L PG.38
Charge PG.35
Dis-Charge PG.39
+VGACORE PG.42
+1.5 VGA PG.43
+1.0V/+1.8/ +3 VGA PG.44

SODIMM1 Max. 4GB PG.12 — 1600MT/s DDR3 L Channel A

SODIMM2 Max. 4GB PG.13 — 1600MT/s DDR3 L Channel B

INTEL Haswell
Processor : Daul / Quad Core
Power : 37 / 47 (Watt)
Package : rPGA947
Size : 37.5 x 37.5 (mm)
PG.2~5

PCI-E x8

AMD
Mars / SUN XT
29mm X 29mm
TDP 35W / 25W
PG.14~20

DDR3 900MHz

VRAM
128Mx16x8,128bit PG.21~22

eDP (5.4Gb/s)

DDI (5.4Gb/s)

FDI DMI

HDD PG.33 — SATA0

ODD PG.33 — SATA1

INTEL PCH
Lynx Point
Power : 3.5 Watt
Package : FCBGA695
Size : 20 x 20 (mm)
PG.6~11

eDP — RTD 2136 S/R DP to LVDS Converter PAGE 23 — LVDS Interface PG.25 — LVDS

DP Port B — HDMI PG.26

CRT — CRT PG.25

PCI-E x 1 LANE2 LANE1

LAN RTL8166EH 10/100 PG.30

WLAN BT COMBO PG.34 — USB 2.0 PORT10

USB 3.0 — USB3.0 Ports X2 PG.29 — Webcam PG.25

USB 2.0 PORT1,2 PORT4 PORT0,1

USB2.0 Ports PG.29

PCI-E x 1 LANE3

Accelerometer PG.34 — SMBUS

Card Reader RTS5237 PG.27

KBC EnE KB3940QF A1 PG.31 — LPC

KB PG.32 | TP PG.32 | ROM PG.31 | FAN PG.32

AUDIO CODEC ALC 3227 PG.28

Speaker PG.28

HP/MIC PG.29

Analog MIC PG.29

Stackup
TOP
GND
IN1
IN2
VCC
BOT

NB5

PROJECT : R63
Quanta Computer Inc.

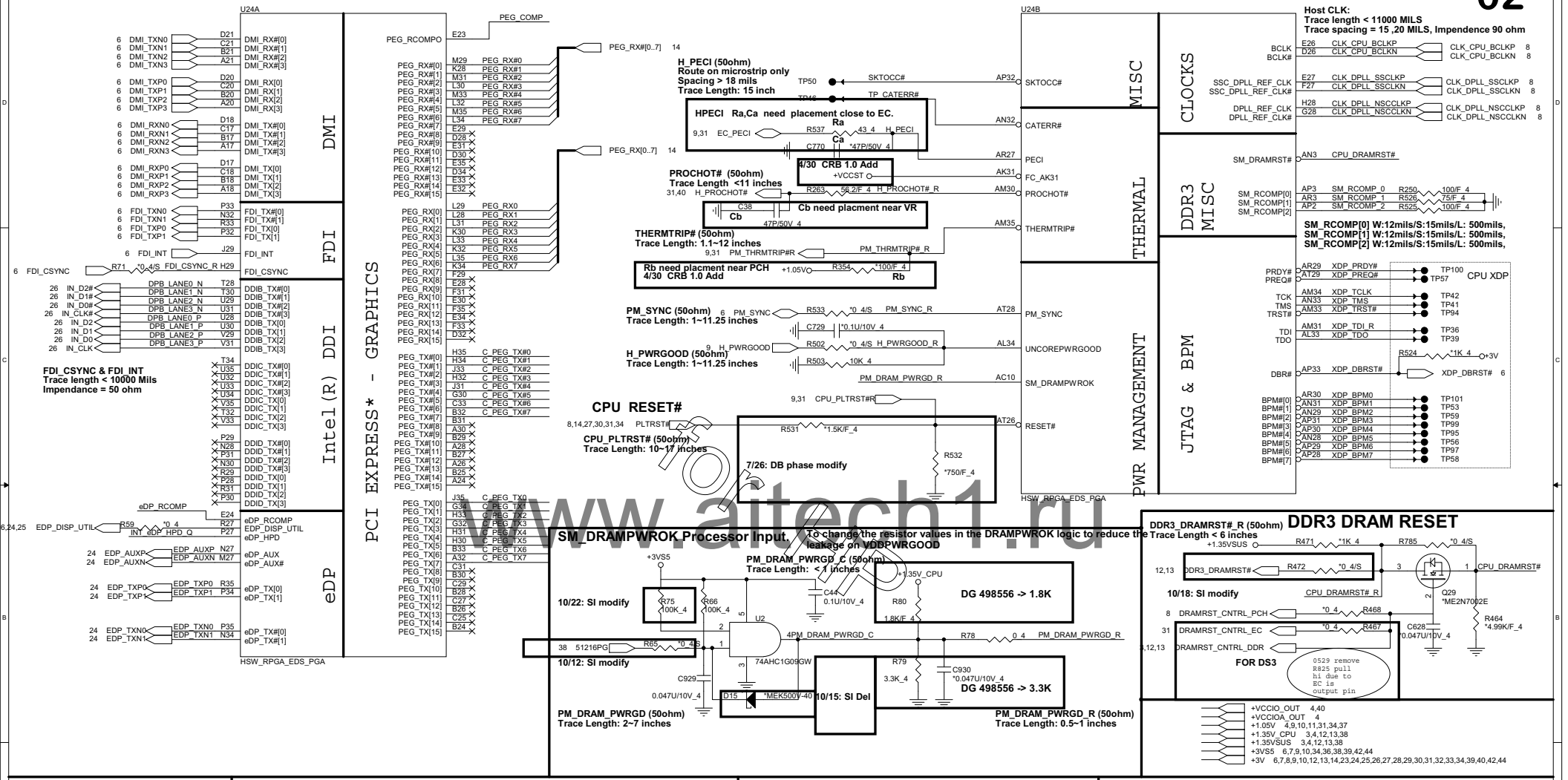
Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Friday, December 21, 2012 Sheet 1 of 44

Haswell Processor (DMI,PEG,FDI)

Haswell Processor (CLK,MISC,JTAG)

02



SM_DRAMPWROK Processor Input.

To change the resistor values in the DRAMPWROK logic to reduce the leakage on VDDPWRGOOD

PM_DRAM_PWRGD_C (50ohm)
Trace Length: < 1 inches

10/22: SI modify

DG 498556 -> 1.8K

10/12: SI modify

10/15: SI Del

DG 498556 -> 3.3K

PM_DRAM_PWRGD (50ohm)
Trace Length: 2~7 inches

PM_DRAM_PWRGD_R (50ohm)
Trace Length: 0.5~1 inches

DDR3 DRAM RESET

DDR3_DRAMRST#_R (50ohm)
Trace Length < 6 inches

10/18: SI modify

FOR DS3

0529 remove R825 pull hi due to EC is output pin

+VCCIO_OUT 4,40
+VCCIOA_OUT 4
+1.05V 4,9,10,11,31,34,37
+1.35V_CPU 3,4,12,13,38
+1.35VSUS 3,4,12,13,38
+3VS5 6,7,9,10,34,36,38,39,42,44
+3V 6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44

4/30 CRB V1.0 -> 10K

PEG x8 disable (UMA only remove)

0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

eDP_RCOMP
Trace length < 100 Mils
Trace Width 20 Mils Trace Spacing 25 Mils

PEG_RCOMP
Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS

Processor pull-up (CPU)

check

PROJECT : R63
Quanta Computer Inc.

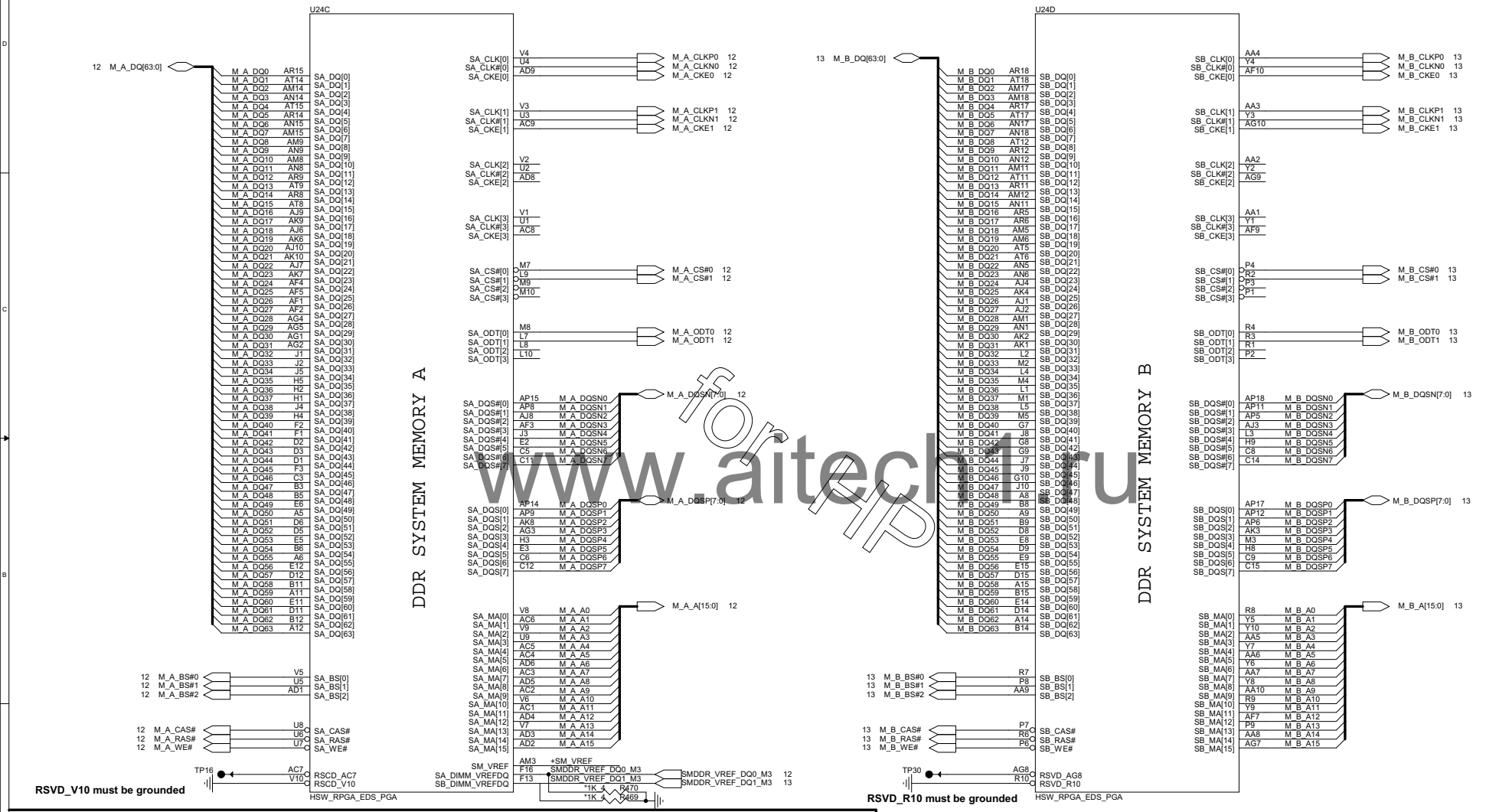
NB5

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A

Date: Friday, December 21, 2012 | Sheet 2 of 44

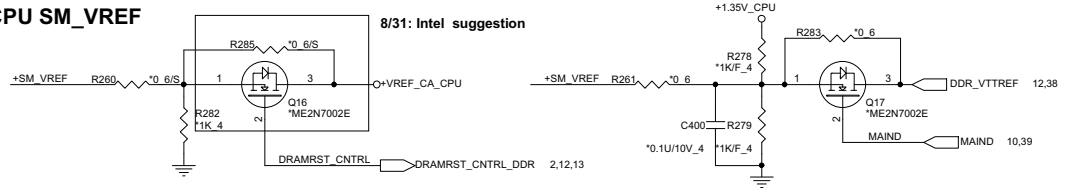
Haswell Processor (DDR3)

03



CPU SM_VREF

8/31: Intel suggestion



+1.35V_CPU 2,4,12,13,38
+VREF_CA_CPU 12

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: SNB 2/4 (DDR3 I/F)	Rev: 1A
Date: Friday, December 21, 2012	Sheet 3 of 44	

Haswell Processor (POWER)

04

POWER

U24F

+VCCIN 95A

+1.35V_CPU 4.2A

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

HSW_RPGA_EDS_PGA

VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

+VCCIOA_OUT 2
+VCCIO_OUT 2,40
+VCCIO_PCH 10
+1.5V 6,7,8,10,28,34,38,44
+1.35V_CPU 2,3,12,13,38
+1.05V 2,9,10,11,31,34,37
+VCC_CORE 40,41
+VCCST 2
+1.35VSUS 2,3,12,13,38

IO Thrm Protect

+3VPCU

For 65 degree, 1.8v limit, (SW)

R774 16.5K/F_4

THRM_MOINTOR 31

C62 0.1U/10V_4

R775 3.3K/F_4

For 75 degree, 1.2v limit, (HW)

THRM_MOINTOR1 31

R776 100K_4 NTC

C54 0.1U/10V_4

4/30: CRB 1.0 add

+1.05V R256 *0_8 +VCCST

C392 *22U/6.3VS_8

C381 *22U/6.3VS_8

Power Test Propose

+1.05V R60 150/F_4 PWR_DEBUG_R R62 *10K_4

+1.05V +VCCIO_OUT R510 *0_8 C753 10U/6.3V_6

+1.05V +VCCIO_PCH R462 0_6 CRB 1.0 stuff C631 *4.7U/6.3V_6

4/30: DG 498550

Haswell PWR_DEBUG requires a 150-Ohm pull-up resistor to PCH 1.05-V VCC Core when routed to XDP

SVID CLK

Layout note: It is recommended to shield VIDSOUT signal by routing it in between the VIDSCLK and VIDALERT# signals.

H_CPU_SVIDCLK VR_SVID_CLK 40

SVID DATA

7/26: DB sch modify, Del R23

+VCCIO_OUT R253 130/F_4

Place PU resistor close to CPU

Place PU resistor close to VR

DG V0.7 -> 110 Ohm
SCH V0.7 -> 130 Ohm

H_CPU_SVIDDAT VR_SVID_DATA 40

SVID ALERT

Place PU resistor close to CPU
The VIDALERT# signal must have a damping resistor to prevent overshoot

C337 0.1U/10V_4

+VCCIO_OUT R247 75/F_4

H_CPU_SVIDALRT# R248 43_4 VR_SVID_ALERT# 40

DG V0.7 -> 44 Ohm
SCH V0.7 -> 43 Ohm

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

CPU VDDQ

+1.35V_CPU +1.35VSUS

Placement close to CPU.

C235 0.1U/10V_4

C225 *0.1U/10V_4

Note: please keep plane is enough for VDDQ 4.2A

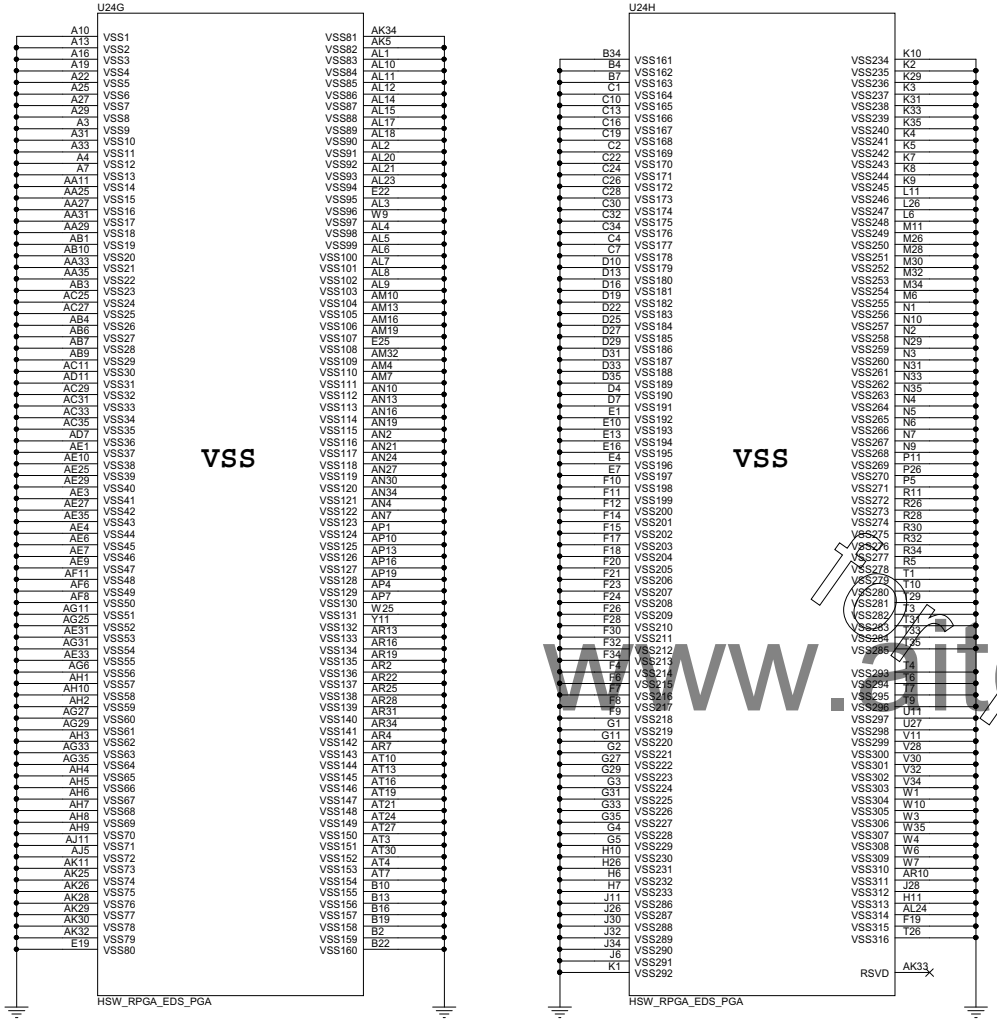
NB5

PROJECT : R63
Quanta Computer Inc.

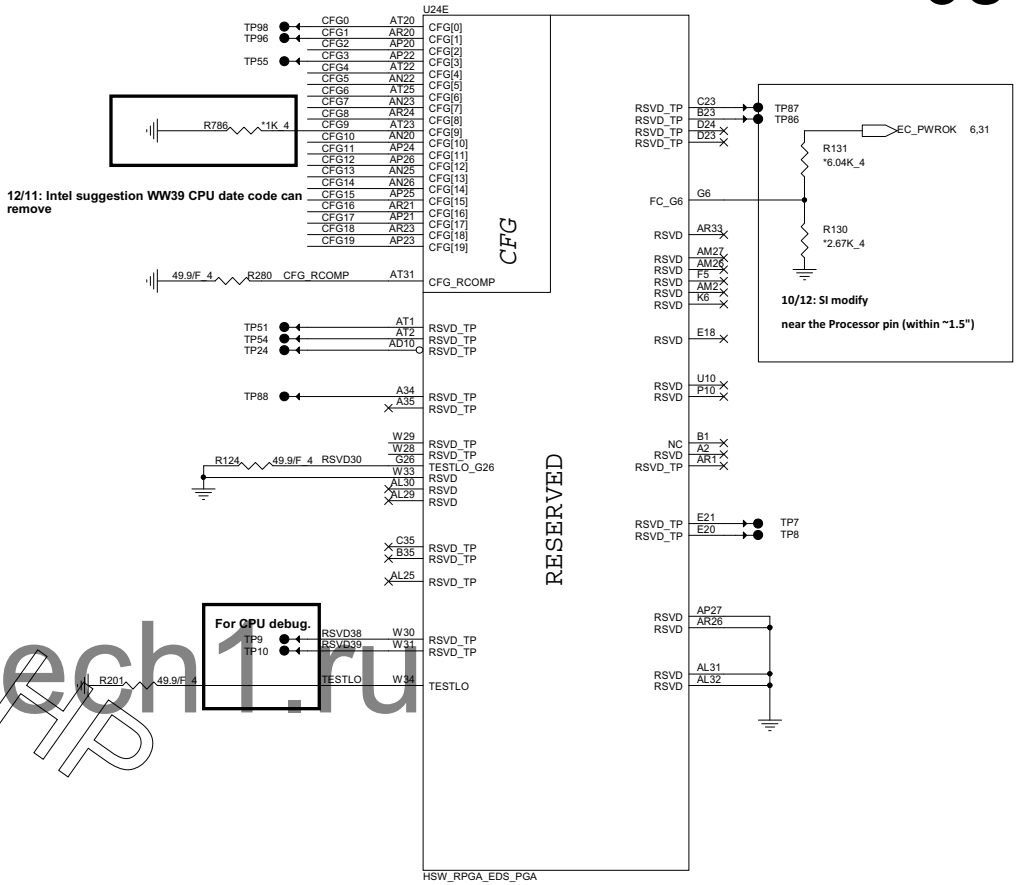
Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A

Date: Friday, December 21, 2012 Sheet 4 of 44

Haswell Processor (GND)



Haswell Processor (RESERVED, CFG)



CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

CFG3 R272 *1K_4

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG2 R275 *1K_4
CFG4 R271 1K_4
CFG7 R273 *1K_4
CFG5 R274 1K_4
CFG6 R270 *1K_4

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: SNB 4/4 (GND)	Rev: 1A
Date: Friday, December 21, 2012	Sheet 5 of 44	

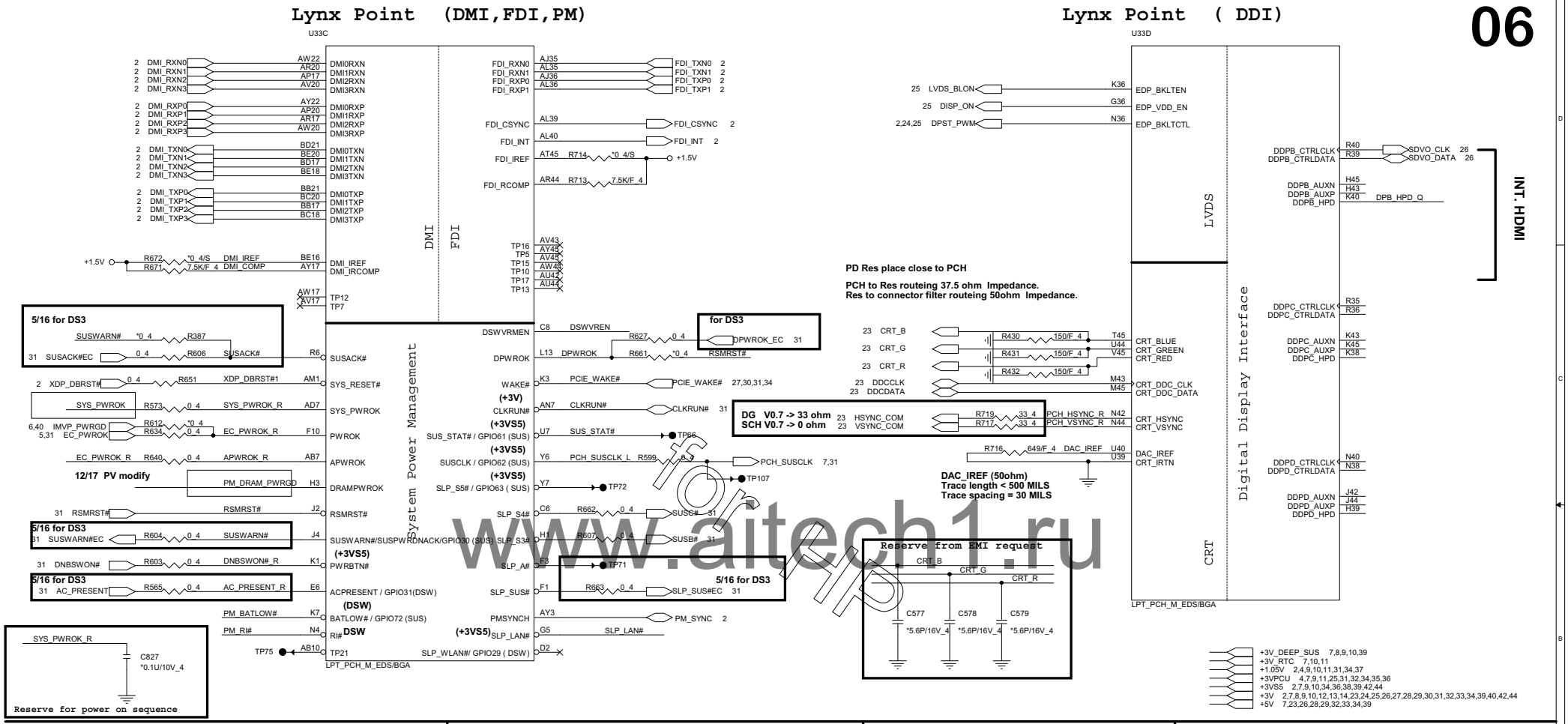
Lynx Point (DMI,FDI,PM)

U33C

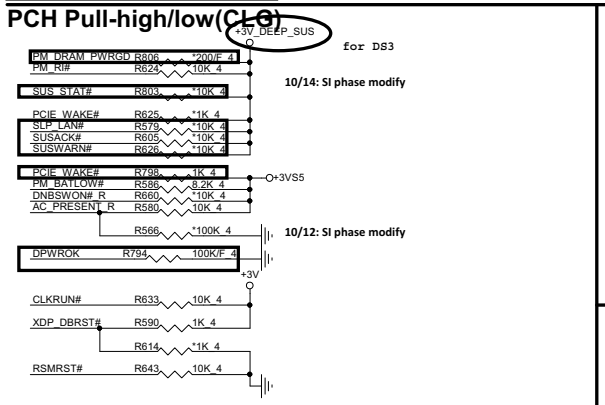
Lynx Point (DDI)

U33D

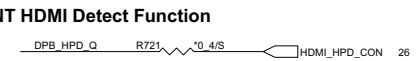
06



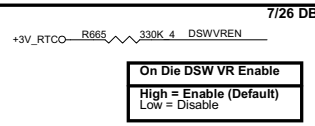
PCH Pull-high/low(CLG)



INT HDMI Detect Function

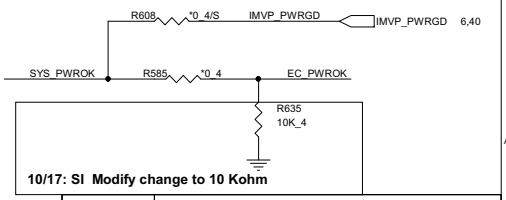


7/26 DB Modify



System PWR_OK(CLG)

7/26 DB Modify



PROJECT : R63
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A

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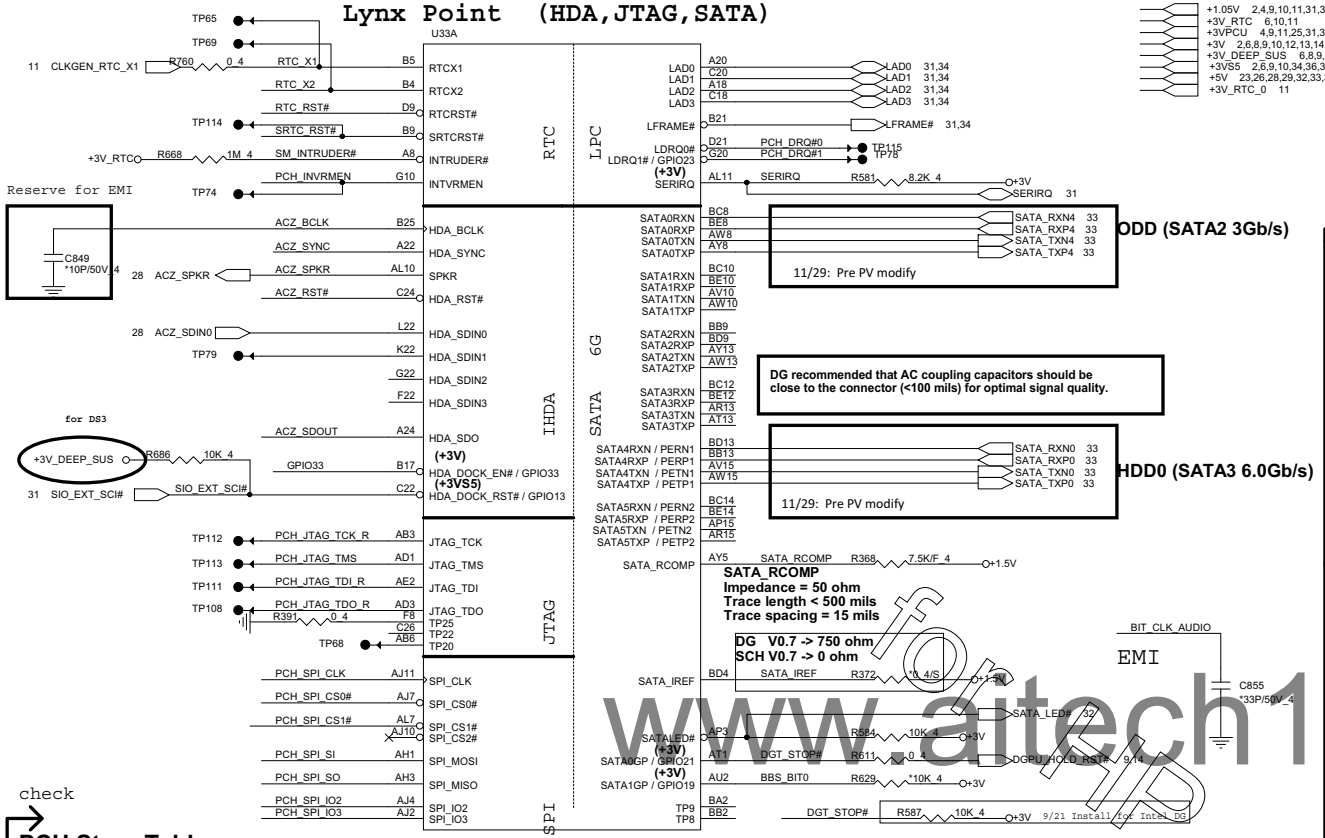
Lynx Point (HDA,JTAG,SATA)

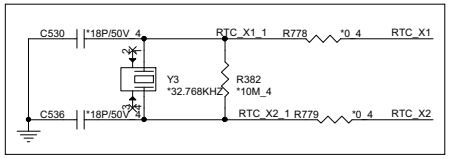


+1.05V 2,4,9,10,11,31,34,37
+3V_RTC 6,10,11
+3VPCU 4,9,11,25,31,32,34,35,36
+3V 2,6,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
+3V_DEEP_SUS 6,8,9,10,39
+3VS5 2,6,9,10,34,36,38,39,42,44
+5V 23,26,28,29,32,33,34,39
+3V_RTC_0 11

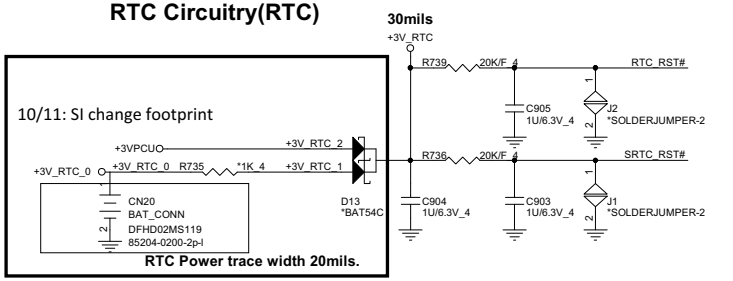
10/18: SI Modify

RTC Clock 32.768KHz

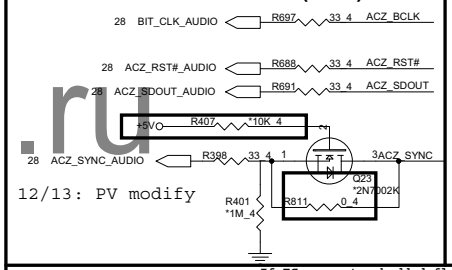
07



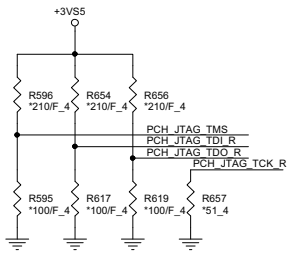
RTC Circuitry(RTC)



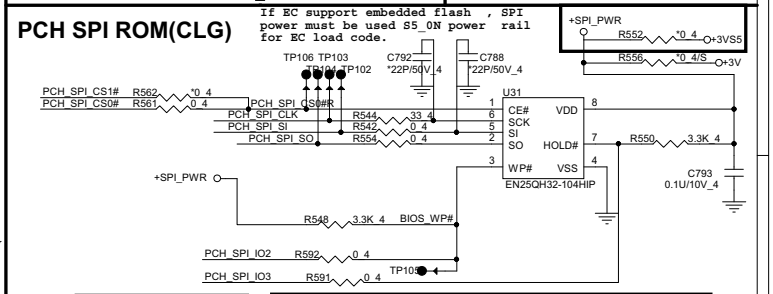
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



10/18: Del R350 , R344

Vender	Size	P/N
EON	4MB	AKE39ZN0Q03 EON EN25QH32-104HIP
AMIC	4MB	AKE39ZN0800 AMIC A25QE32M-F (QE)
Socket		DFHS08FS023

check

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R569 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (Int PU)	R563 *1K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Disable 1 = Enable	PCH_INVRMEN R389 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R680 *0_4 +3V 10/18: SI Modify
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 1 SPI; 0 0 LPC	[Need external pull-down for LPC BIOS] Default weak pull-on GNT0/1#
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R613 *1K_4 BBS_BIT0 R390 *1K_4 BBS_BIT1 8
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+VCC_HDA_IO R684 *1K_4 ACZ_SYNC 12/13: PV modify
HDA_SDO	Flash Descriptor Security	PWROK	0 = Security Effect (Int PD) 1 = Can be Overridden	31 GPIO33_E ACZ_SDOUT R693 *1K_4 +VCC_HDA_IO
GPIO8	RSVD	RSMRST#	Internel PU	R621 *1K_4 BT_OFF# 9,34
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Int PU)	R571 *1K_4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R374 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	R564 *1K_4 PCH_SUSCLK 6,31

LPT_PCH_M_EDS/BGA

PROJECT : R63
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A
Date: Monday, December 24, 2012	Sheet 7 of 44	

08

Lynx Point (PCI,USB,NVRAM)

Lynx Point (PCI-E,SMBUS,CLK)

PCI/USBOC# Pull-up(CLG)

USB3.0

PLTRST#(CLG)

7/26 DB modify

SMBus/Pull-up(CLG)

12/18 PV modify

PEG Clock detect (SG only)

7/26 DB modify

CLK_REQ/Strap Pin(CLG)

7/26 DB modify

PCIE Clock

SMBus/Pull-up(CLG)

check

MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

4/30: CRB 1.0 =>rename PCH_TP26

12/11: PV modify

10/12: SI modify

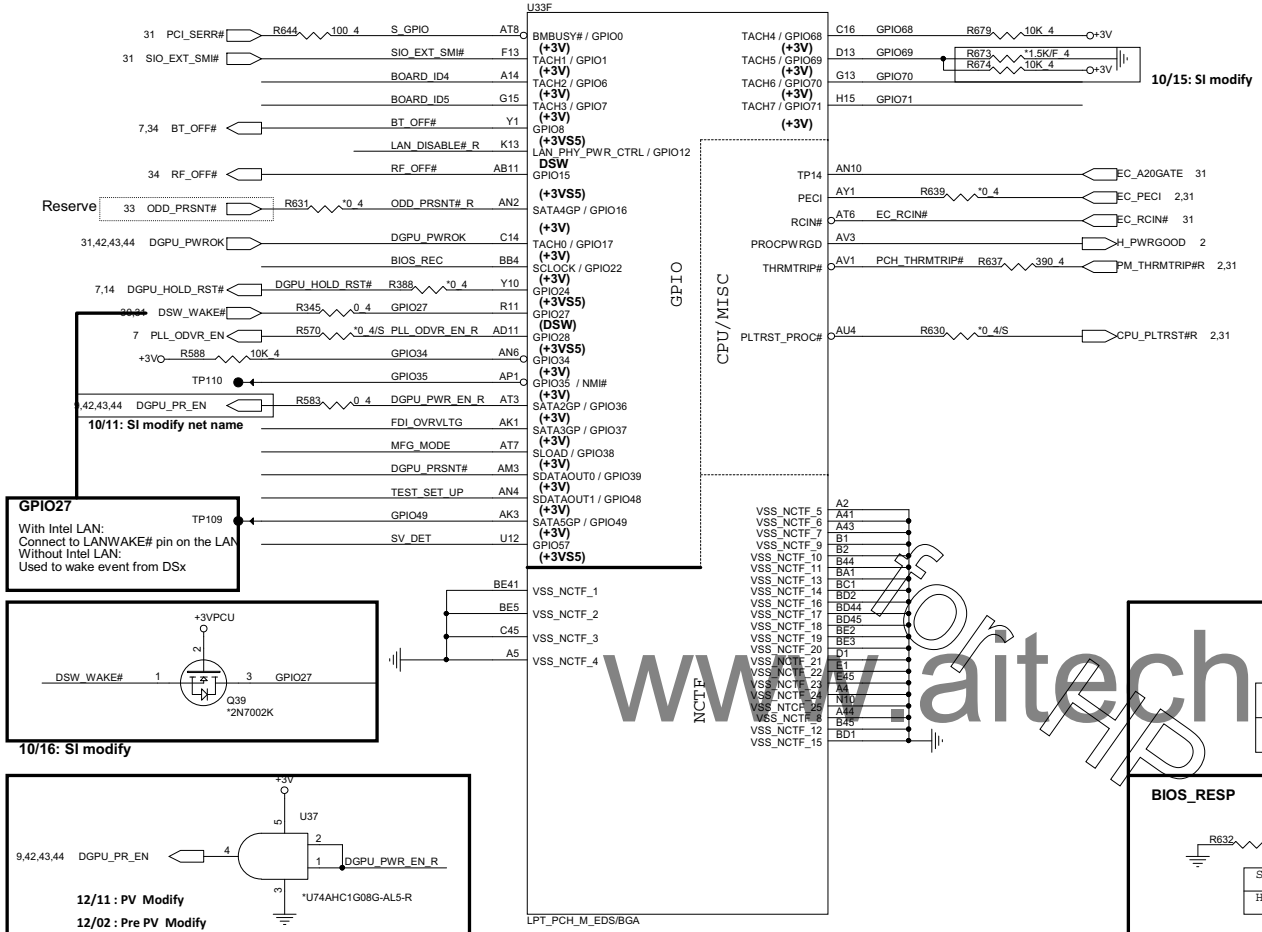
10/18: SI modify

change 25M to small size

Remove for UMA only.

PROJECT :	R63
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: PCH 3/6 (PCIE/USB/CLK)
Rev: 1A	
Date: Monday, December 24, 2012	Sheet 8 of 44

Lynx Point (GPIO,VSS_NCTF,RSVD)

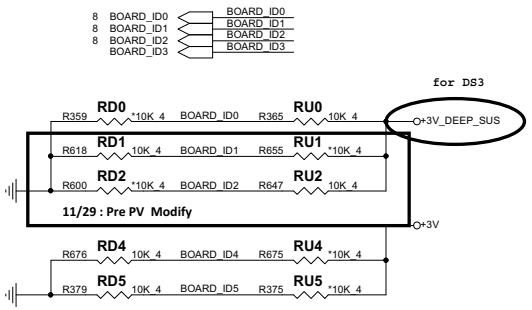


10/16: SI modify

12/11 : PV Modify
12/02 : Pre PV Modify

BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4		BOARD_ID2	BOARD_ID1	BOARD_ID0
DB R63 UMA				0	0	0
DB R63 DIS				0	0	1
SI R63 UMA				0	0	0
SI R63 DIS				0	0	1
PV R63 UMA				1	0	0
PV R63 DIS				1	0	1



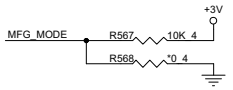
Clock Gen Power OK (CLG)

+3V_DEEP_SUS 6,7,8,10,39
+3VS5 2,6,7,10,34,36,38,39,42,44
+3V 2,6,7,8,10,12,13,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
+5VS5 23,29,30,34,36,37,38,39,40,41,42,43,44

09

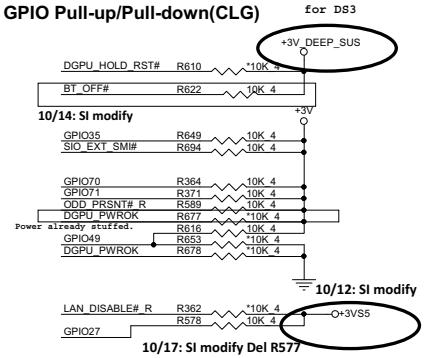
PCH MISC PU /PD

MFG-TEST



GPIO Pull-up/Pull-down(CLG)

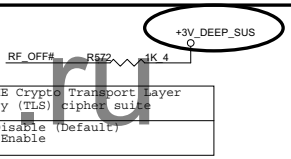
for DS3

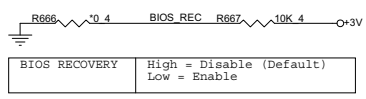


Swap GPIO

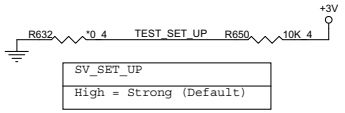
0 = SGPIO
1 = Default

for DS3





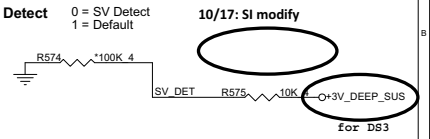
BIOS_RESP



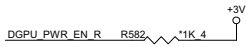
SV Detect

0 = SV Detect
1 = Default

10/17: SI modify



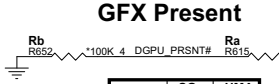
GPIO36 Internal PD



SATA3GP/GPIO37 TLS Confidentiality

0 = TLS no confidentiality (Int PD)
1 = TLS with confidentiality

GFX Present



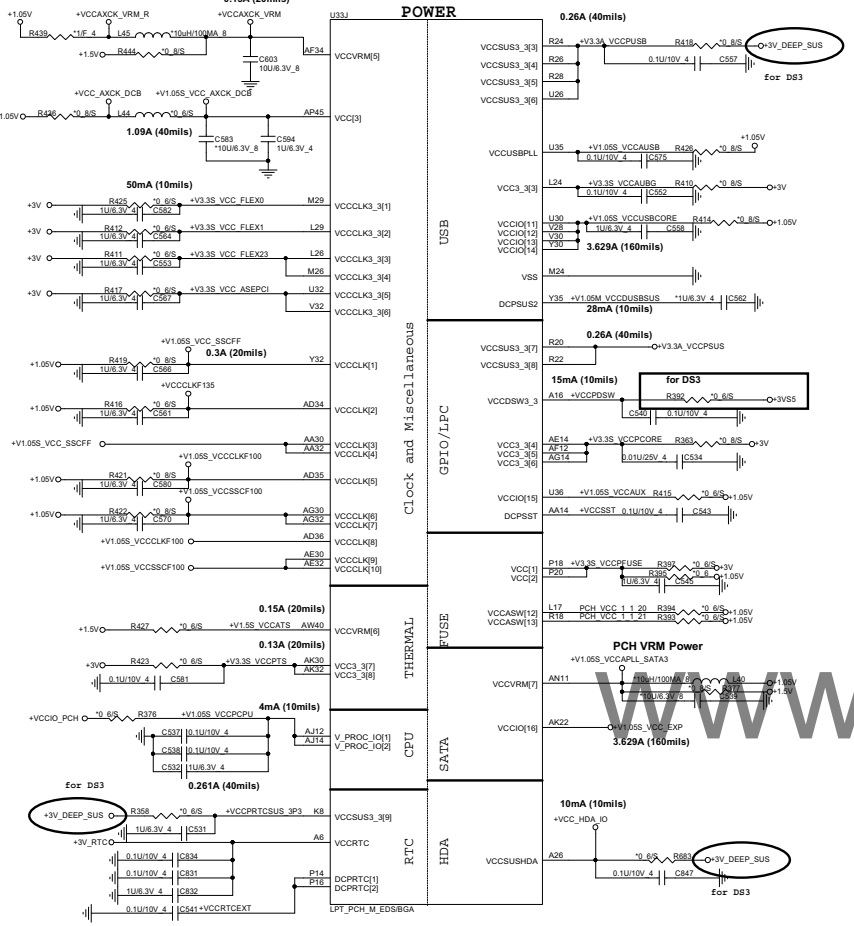
	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

NB5

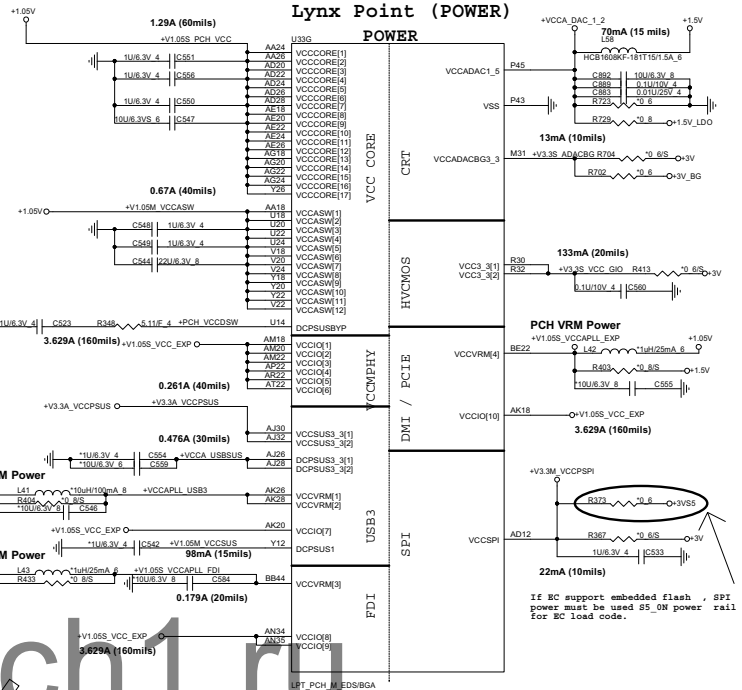
PROJECT : R63
Quanta Computer Inc.

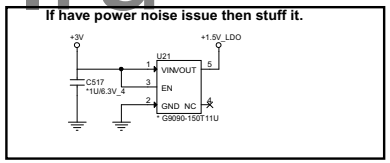
Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
Date: Monday, December 24, 2012	Sheet 9 of 44	

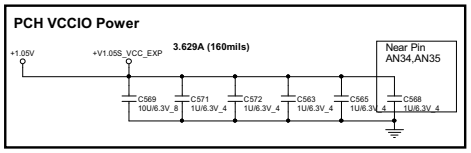
Lynx Point (POWER)

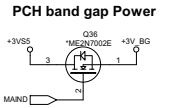


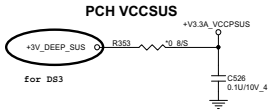
Lynx Point (POWER)

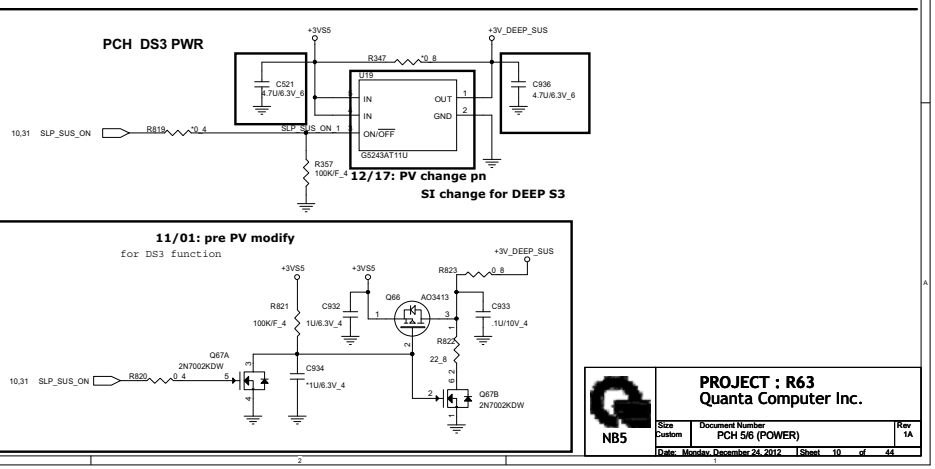






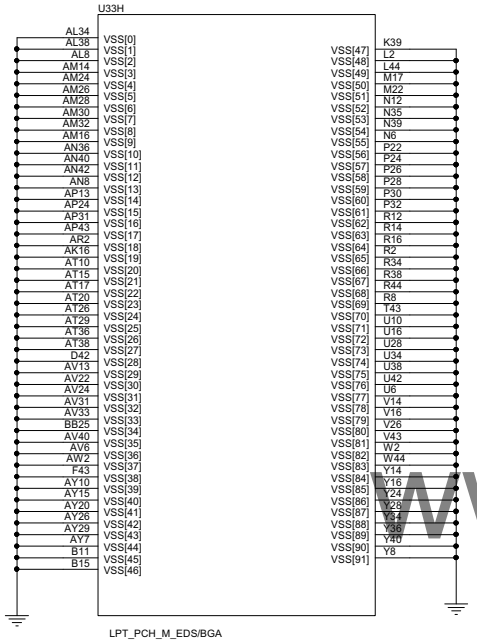




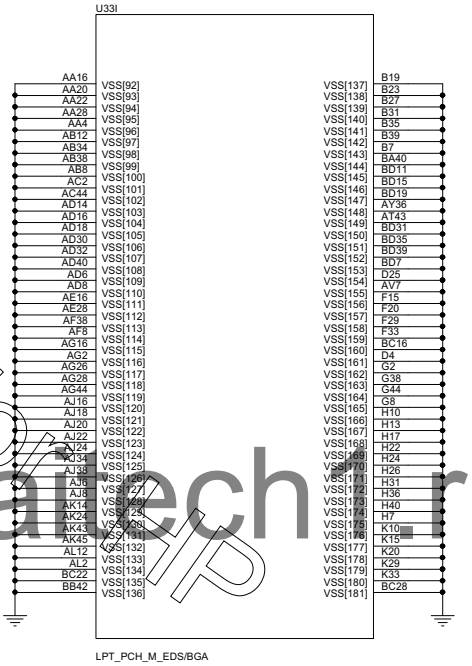


NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: PCH 5/6 (POWER)	Rev: 1A
Date: Monday, December 24, 2012	Sheet 10 of 44	

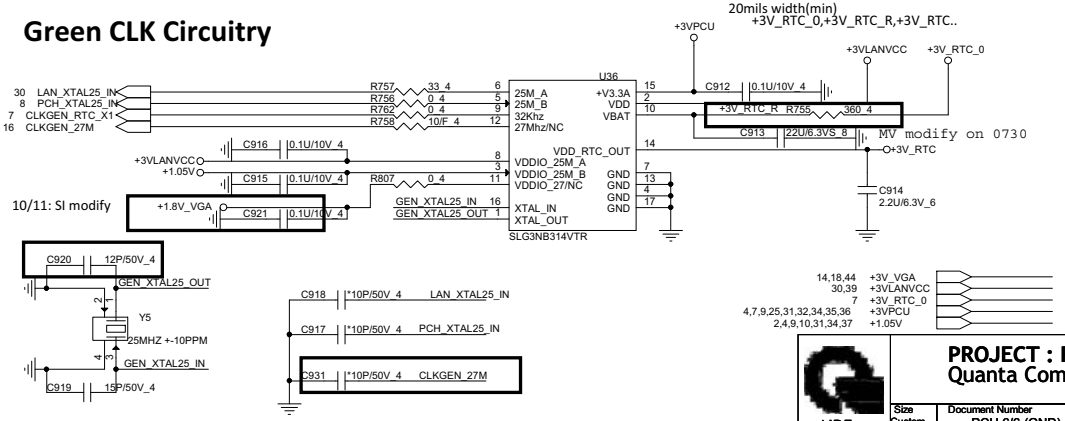
Lynx Point (GND)



Lynx Point (GND)



Green CLK Circuitry



	U36 P/N
UMA	AL3NB244000
DIS	AL000314000

NB5	PROJECT : R63 Quanta Computer Inc.
Size: Custom	Document Number: PCH 6/6 (GND) — Rev: 1A
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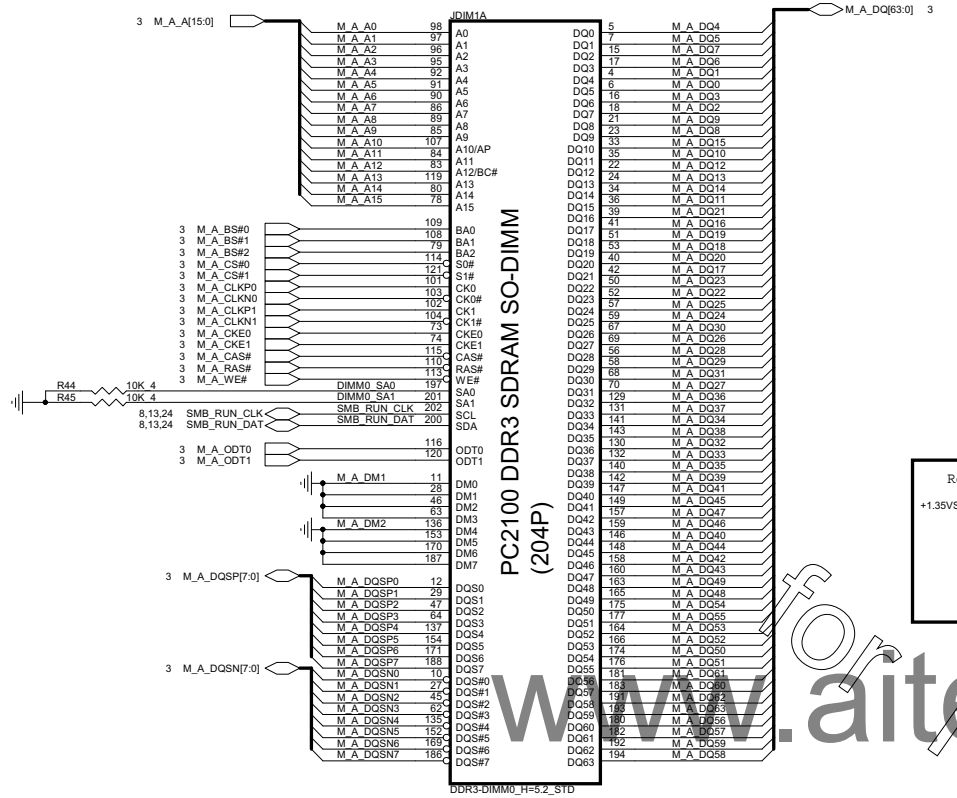
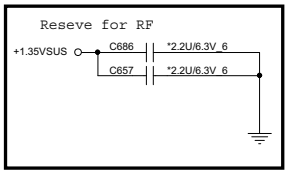
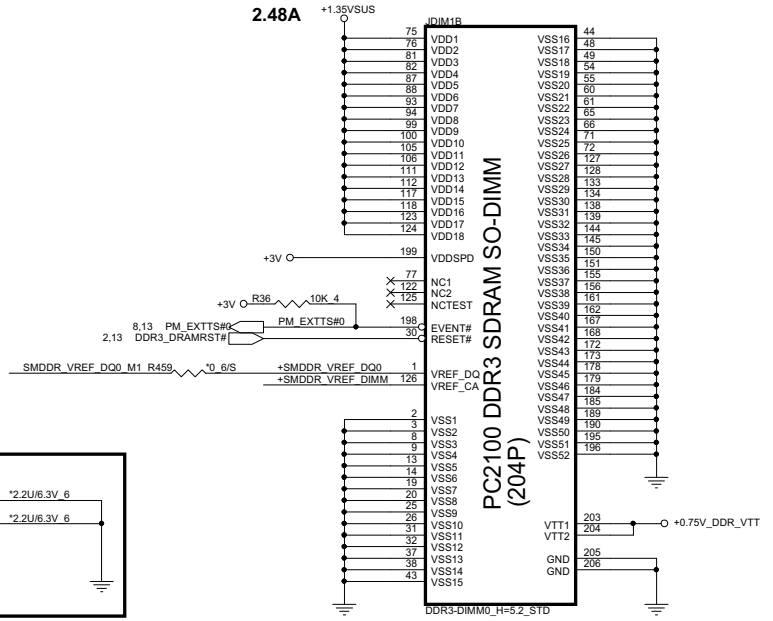
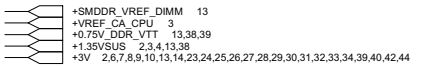
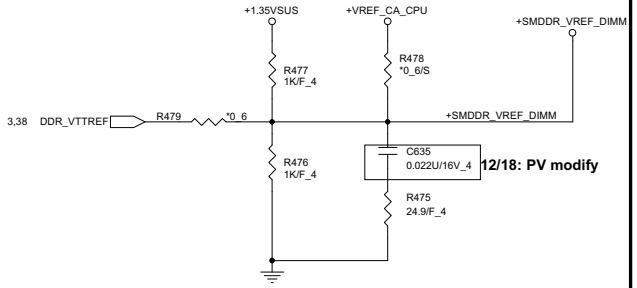




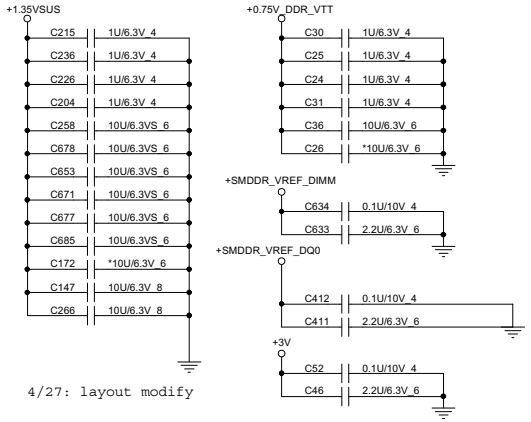
2.48A







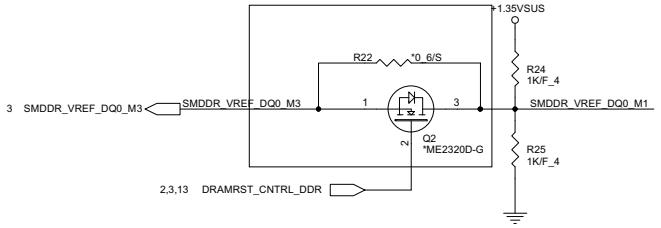
Place these Caps near So-Dimm0.



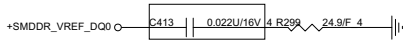
4/27: layout modify

VREF DQ0 M1 Solution

8/31: Intel suggestion



10/17: SI modify



NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A

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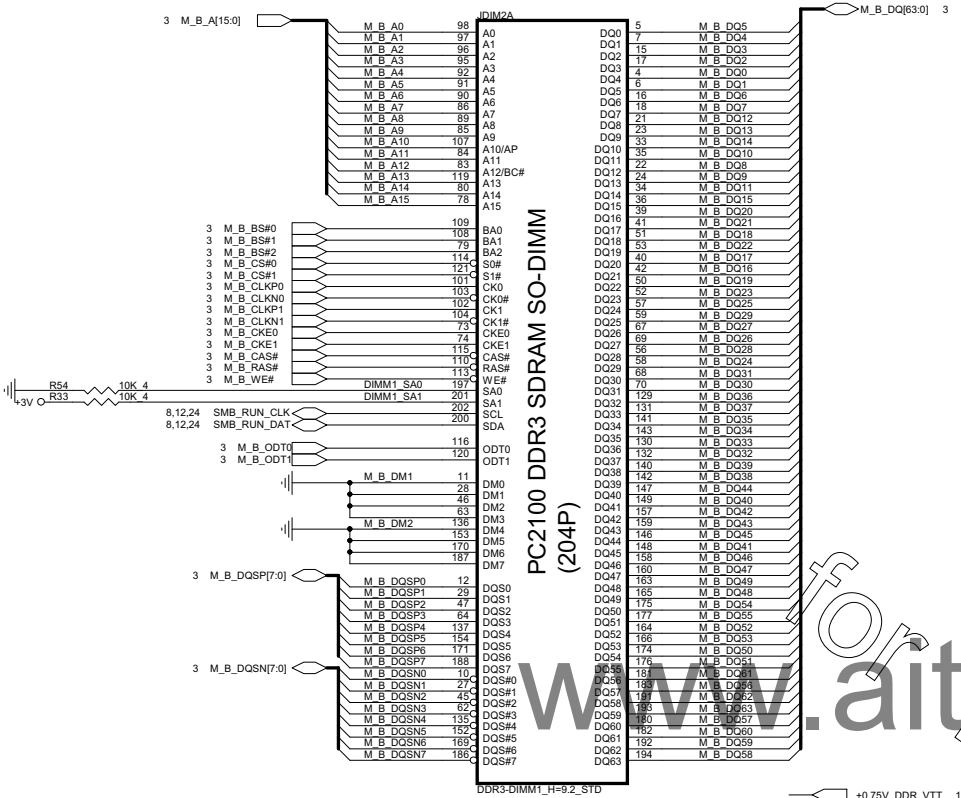
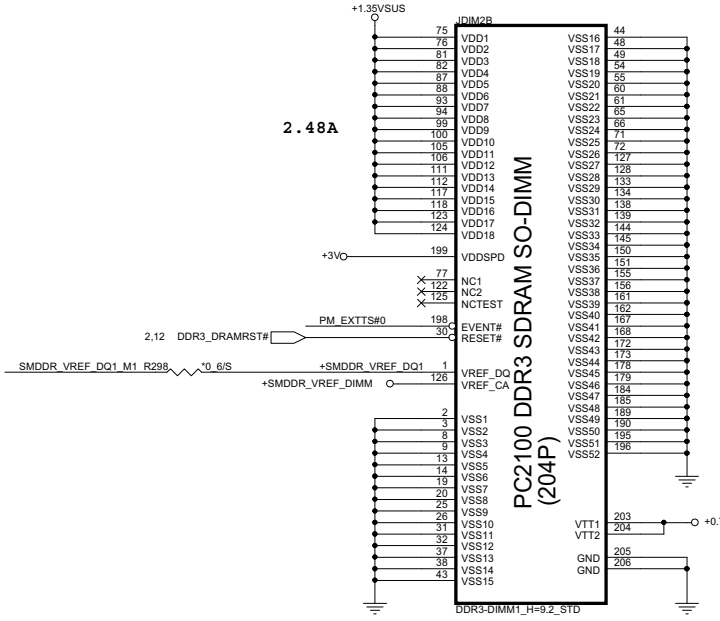
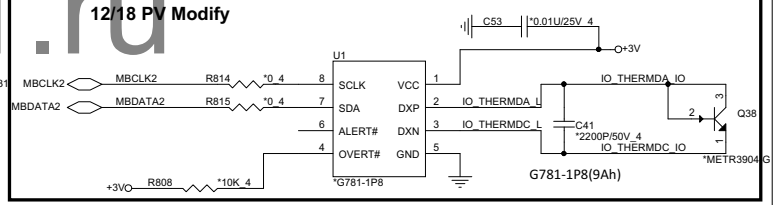




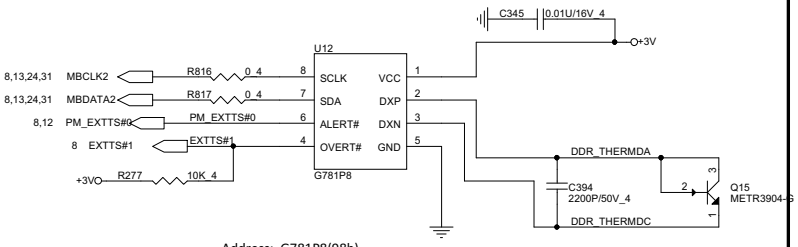
+0.75V_DDR_VTT 12,38,39
+1.35VSUS 2,3,4,12,38
+3V 2,6,7,8,9,10,12,14,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44
+SMDDR_VREF_DIMM 12

Local Thermal Sensor

12/18 PV Modify

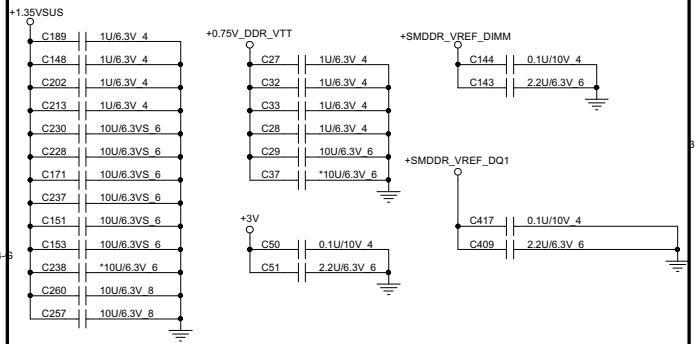


DDR Thermal Sensor

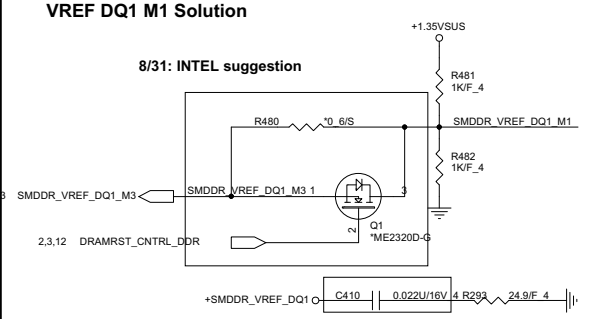


Address: G781P8(98h)

Place these Caps near So-Dimm1.

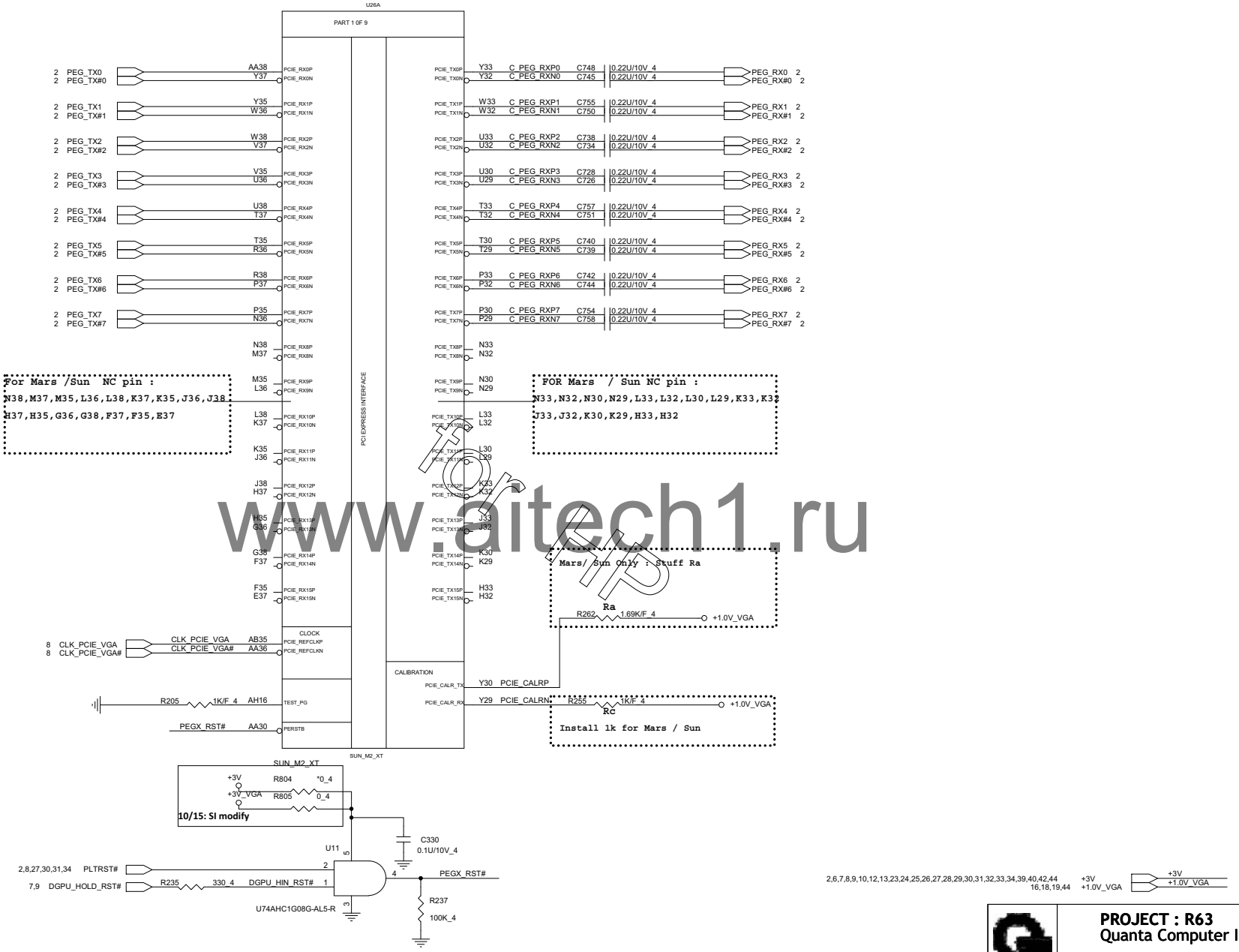


VREF DQ1 M1 Solution



PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A
NB5	Date: Friday, December 21, 2012	Sheet 13 of 44



2,6,7,8,9,10,12,13,23,24,25,26,27,28,29,30,31,32,33,34,39,40,42,44 +3V
16,18,19,44 +1.0V_VGA

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: THAMES_PCIE_Interface	Rev: 1A
Date: Friday, December 21, 2012	Sheet 14 of 44	

For Mars / Sun : AR1/AW8/AR3/AR8/AU8: NC pin

For Sun only : AD29 /AC29 /AJ21 /AK21: NC pin

For Mars / Sun : DP A to D Port: all NC pin

For Sun only :
AP10 /AV11 /AT11 /AR12 /AW12 / AU12 /AP12 : NC pin

10/17: SI modify

12/13: PV modify

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

8/24: DB Modify

A 3-k external pull up (3.3 V) is required if an external BIOS ROM chip is used.

FOR SUN GPIO NC PIN : AJ19/ AK19 / AK24 / AM14 / AN14 / AJ24/ AH26 / AH24 / AJ20

AK20/ AH18 / AN16 / AK17 / AK16 / AL16/ AM16

Mars: stuff

For Sun Nc: R167, R141, C155

10/14: SI modify

FOR MARS: AD37/ AE38 / AD35 AVSSN to GND
FOR SUN : AD37/ AE38 / AD35 NC pin

8/15 DB Modify

10/14 SI Modify

DEL R747 R748 R749

10/14: SI modify , DEL R751, R753

FOR SUN NC PIN : AD34/ AE34 / AC33 / AC34 / AD39 / AE36

AF37/ AC36 / AC38 / AB34 /

MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table:

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

PS_0[3:1]	romiddfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romiddfg[2:0] define memory aperture size If bios_rom_en = 1, romiddfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

BIT5 => BIT1

PS0	=>	11001
PS1	=>	00001
PS2	=>	00000
PS3	=>	11000

VENDOR	R231	R232
HYNIX 2G	NA	4.75K
MICRON 2G	8.45K	2K
SAM 2G	4.53K	2K
HYNIX 1G	6.98K	4.99K
MICRON 1G	4.53K	4.99K
SAM 1G	3.24K	5.62K

Thermal Solution(Close to GPU)

12/13: PV modify

Address: G781-1P8(9Ah)

Reserve for Power Play

For Mars: Stuff Ra, Rc=> VDDC 1.1V

For Mars / Sun:NC pin
AL30, AM30, AL29, AM29, AN21, AM21, AK30, AK29

For Sun Only :NC pin
AL27, AM27, AM20, AN20, AN26, AM26, AL19, ,
AM19, AJ30, AJ31

PS3 BIT3->BIT1	ID
000	0
001	1
010	2
011	3
100	4
101	5

Memory Type	Configuration	PN	Channel Size

14,16,18,19,44 +1.0V_VGA → +1.0V_VGA
11,16,18,19,44 +1.8V_VGA → +1.8V_VGA
17,18 +3V_DELAY → +3V_DELAY

NB5

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Quanta Computer Inc.

Size: Custom | Document Number: THAMES_Main & GND | Rev: 1A

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Fo Mars/ Sun
Change La, Lb
Bead to 0 ohm

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

La
+1.8V_VGA L23 *0_6/S +1.8V_DPLL_PVDD
C259 10U/6.3V_8 C264 1U/6.3V_4 C265 0.1U/10V_4
Display Phase Lock Loop Power
DPLL_PVDD : 1.8V @ 75mA

Lb
+1.8V_VGA L21 *0_6/S +1.0V_DPLL_VDDC
1.0V(125mA DPLL_VDDC)
C253 10U/6.3V_8 C269 1U/6.3V_4 C267 0.1U/10V_4
DPLL_PVSS
+1.0V_DPLL_VDDC
DPLL_VDDC : 0.935V @ 140mA

+1.8V_MPLL_PVDD
MPLL_PVDD : 1.8V @ 150mA
+1.8V_VGA HCB1608KF-471T10 L35 +1.8V_MPLL_PVDD
C441 10U/6.3V_8 C437 1U/6.3V_4 C438 0.1U/10V_4

+1.8V_SPLL_PVDD
SPLL_PVDD : 1.8V @ 75mA
+1.8V_VGA L16 FCM1005KF-121T03 +1.8V_SPLL_PVDD
C167 10U/6.3V_8 C176 1U/6.3V_4 C191 0.1U/10V_4

+1.0V_SPLL_VDDC
SPLL_VDDC : 0.935V @ 150mA
+1.0V_VGA L19 HCB1608KF-471T10 +1.0V_SPLL_VDDC
1.0V(125mA DPLL_VDDC)
C181 10U/6.3V_8 C222 1U/6.3V_4 C216 0.1U/10V_4
SPLL_PVSS

DPEF_VDD18
R212 Ra *0_4
R249 Rb *0_4
reserve Ra, Rb for future ASIC

10/14: SI modify

U26I
PART 9 OF 9
AM32 DPLL_PVDD
AN31 DPLL_VDDC
AN32 DPLL_PVSS
H7 MPLL_PVDD
H8 MPLL_PVDD
AM10 SPLL_PVDD
AN9 SPLL_VDDC
AN10 SPLL_PVSS
AF30 NC_XTAL_PVDD
AF31 NC_XTAL_PVSS
PLLS/XTAL
SUN_M2_XT

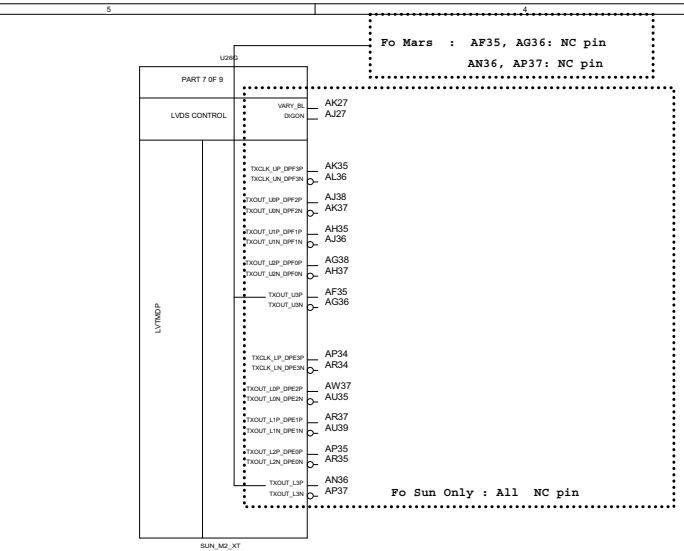
XTALIN AV33 *0_4 R792 EVGA-XTALI
XTALOUT AU34 *0_4 R793 EVGA-XTALO
0_4 R759 CLKGEN_27M 11
R207 *10M_6 Y2 *7A27000010 C244 *22P/50V_4 C245 *22P/50V_4
11/29: Pre PV modify
12/13: PV modify del
XO_IN AW34 TP129
XO_IN2 AW35 R487 *0_4
CLKTESTA AK10 CLKTESTA
CLKTESTB AL10 CLKTESTB
C193 *0.1U/10V_4 C227 *0.1U/10V_4
R477 *51/1%_4 R478 *51/1%_4
Debug only
for clock observation,
if not needed, DNI
route 50ohms
single-ended/
100ohms diff and keep short

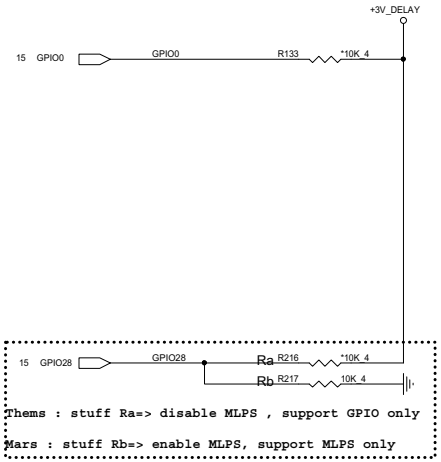
U26F
PART 6 OF 9
AB39 E39 F34 F39 G33 G34 H31 H34 H39 J31 J34 K31 K34 K39 L31 L34 M34 M39 N31 N34 P31 P34 P39 R34 T31 T34 T39 U31 U34 V34 V39 W31 W34 Y34 Y39 PCIE_VSS
F15 F17 F19 F21 F23 F25 F27 F29 F31 F33 F7 F9 G2 G6 H9 J2 J27 J6 J8 K14 K7 L11 L17 L22 L24 L9 M17 M23 M24 N16 N18 N2 N21 N23 N26 N6 R15 R17 R2 R20 R22 R24 R27 R6 T11 T13 T16 T18 T21 T23 T26 U15 U17 U2 U20 U22 U24 U27 U6 V11 V16 V18 V21 V23 V26 W2 W6 Y15 Y17 Y20 Y22 Y24 Y27 GND
A3 A37 AA16 AA18 AA2 AA21 AA23 AA26 AA28 AA6 AB12 AB15 AB17 AB20 AB22 AB24 AB27 AC11 AC13 AC16 AC18 AC2 AC21 AC23 AC26 AC28 AC6 AD15 AD17 AD20 AD22 AD24 AD27 AD9 AE2 AE6 AF10 AF16 AF18 AF21 AG17 AG2 AG20 AG22 AG6 AG9 AH21 AJ10 AJ11 AJ2 AJ28 AJ6 AK11 AK31 AK7 AL11 AL14 AL17 AL2 AL20 AL23 AL26 AL32 AL6 AL8 AM11 AM31 AM9 AN11 AN2 AN30 AN6 AN8 AP11 AP7 AP9 AR5 B11 B13 B15 B17 B19 B21 B23 B25 B27 B29 B31 B33 B7 B9 C1 C39 E35 E5 F11 F13 GND
VSS_MECH A39 AW1 AW39
SUN_M2_XT

AG22 is nc pin

14,18,19,44 +1.0V_VGA +1.0V_VGA
11,15,18,19,44 +1.8V_VGA +1.8V_VGA

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: THAMES_XTAL	Rev: 1A
Date: Friday, December 21, 2012	Sheet 16 of 44	





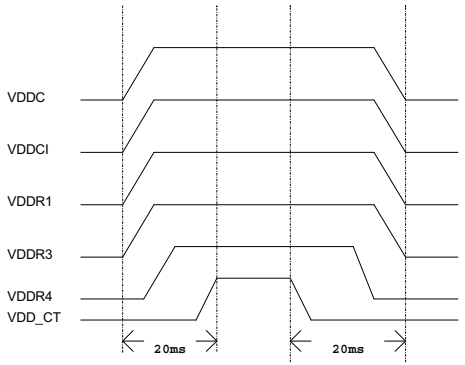
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled, It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0	
0	128M	0	0	0	+VGA_CORE
0	256M	0	0	1	+VGA_CORE
0	64M	0	1	0	+1.5V_VGA
0	32M	0	1	1	+3.3V_Delay
0	512M	1	0	0	+1.8V_VGA
0	1G	1	0	1	+1.8V_VGA
0	2G	1	1	0	
0	4G	1	1	1	

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

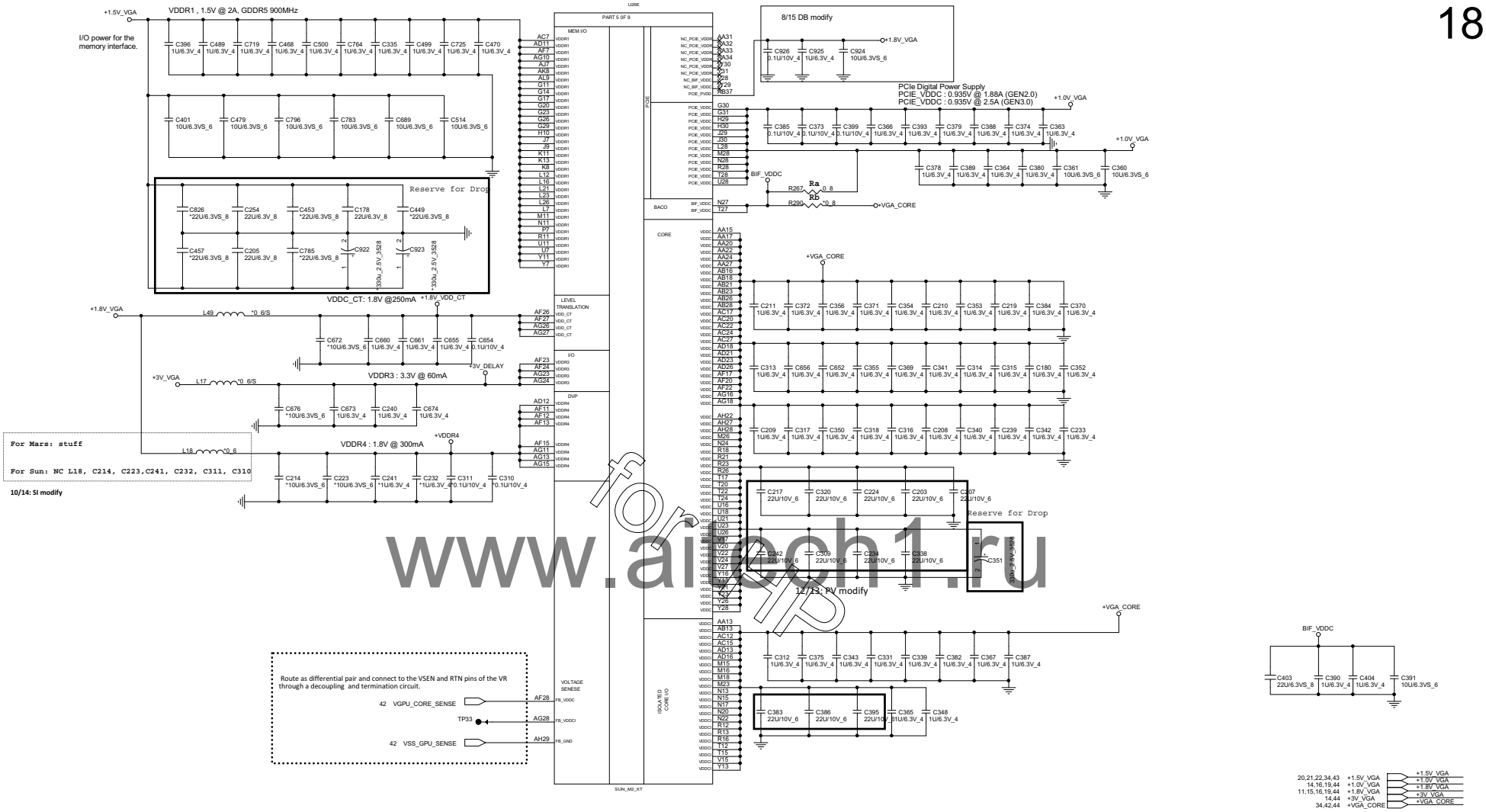
Power Up/Down Sequence



NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_LVDS / STRAP	1A
Date: Friday, December 21, 2012	Sheet 17 of 44	



Support BACO Mode

Notel. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

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NB5	Size: Custom; Document Number: THAMES_Power & BACO; Rev: 1A
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For Mars : L20 sutff

For Sun: L20 , C247 , C246 , C252 NC

+1.0V_VGA

DPAB_VDD10

L20 *0_6

C247 *0.1U/10V_4

C246 *1U/6.3V_4

C252 *10U/6.3VS_6

10/14: SI modify

U26H

PART 8 0F 9

DP_VDDR

DP_VDDC

DP GND

CALIBRATION

SUN_M2_XT

DP_VDDC: AP31, AP32, AN33, AP33

AN24, AP24, AP25, AP26, AU28, AV29 DP_VDDR

DP_VDDC: AP13, AT13, AP14, AP15

DP_VDDC: AL33, AM33, AK33, AK34

AP20, AP21, AP22, AP23, AU18, AV19 DP_VDDR

10/14: SI modify

For Mars : L26 sutff

For Sun: L26 , C279 , C281 , C282 NC

+1.8V_VGA

L26 *0_6

DPEF_VDD18

C279 *10U/6.3VS_6

C281 *1U/6.3V_4

C282 *0.1U/10V_4

AH34, AJ34, AF34, AG34, AM37, AL38 DP_VDDR

10/14: SI modify

DPEF_VDD10

+1.0V_VGA

L25 *0_6

C291 *0.1U/10V_4

C290 *1U/6.3V_4

C293 *10U/6.3VS_6

For Mars : L25 sutff

For Sun : L25/ C293/C290/C291 NC

DP_VSSR: AN27, AP27, AP28, AW24, AW26, AN29, AP29, AP30, AW30, AW32, AN17, AP16, AP17, AW14, AW16, AN19, AP18, AP19, AW20, AW22, AN34, AP39, AR39, AU37, AF39, AH39, AK39, AL34, AV27, AR28, AV17, AR18, AN38, AM35

AW28 DPAB_CALR

AW18 DPCD_CALR

AM39 DPEF_CALR

10/14: SI modify

R495 *150/F_4

For Mars : R495 sutff

For Sun : R495 NC

10/14: SI modify DEL R754

For Mars : R754 sutff

For Sun : R754 NC

14,16,18,44 +1.0V_VGA

11,15,16,18,44 +1.8V_VGA

+1.0V_VGA

+1.8V_VGA

NB5

PROJECT : R63

Quanta Computer Inc.

Size	Document Number	Rev
Custom	THAMES_DP Powers	1A

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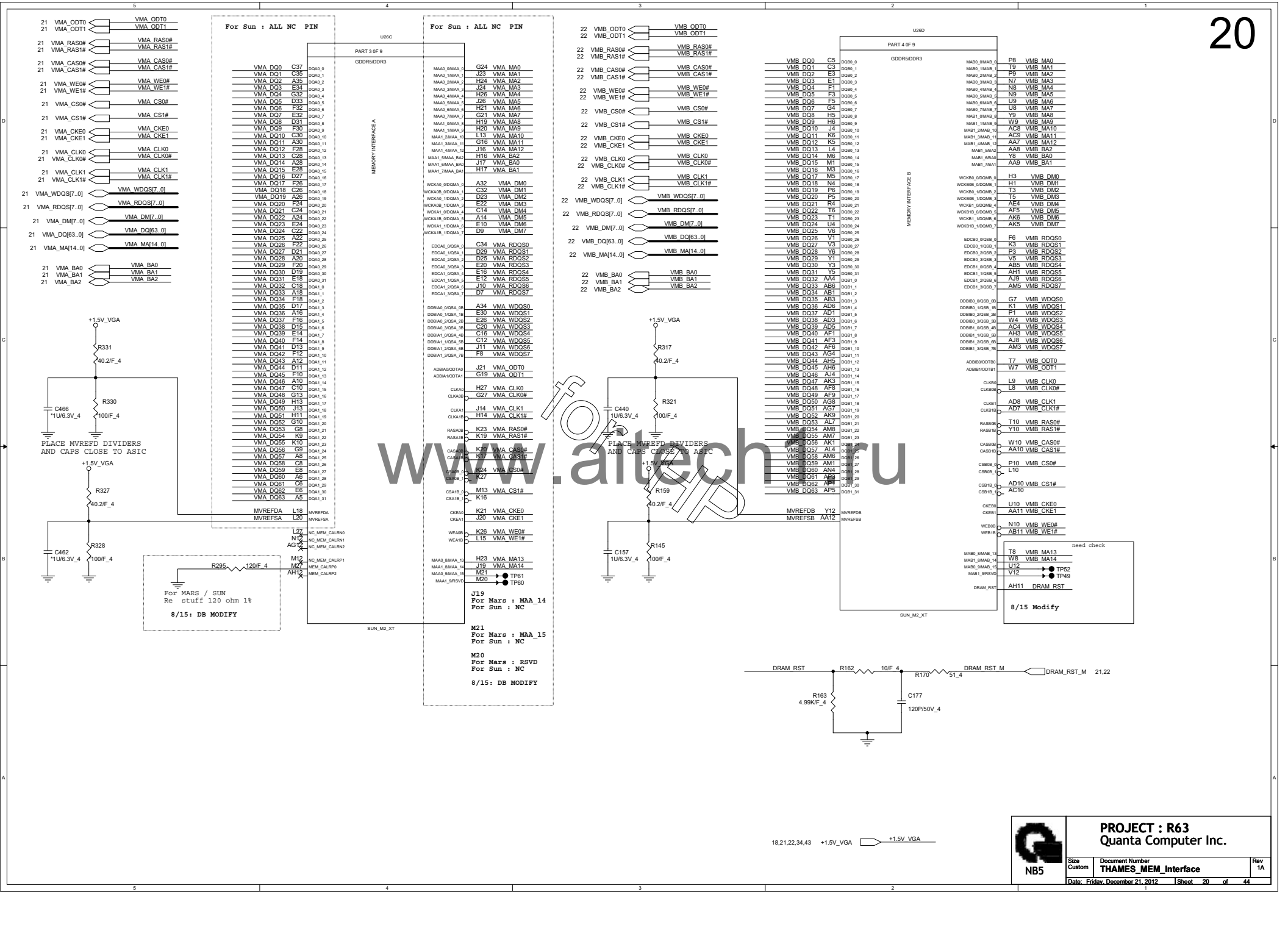
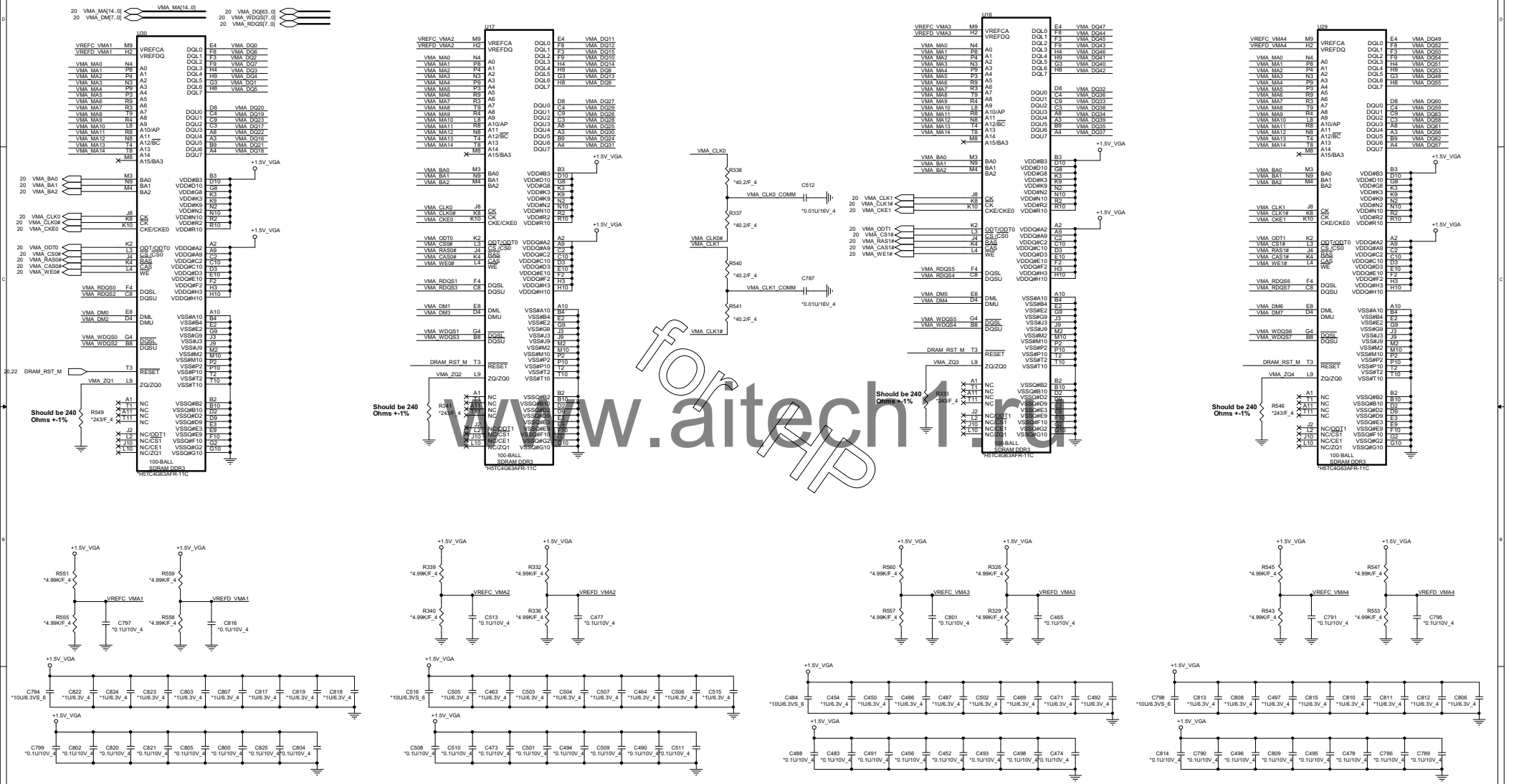


CHANNEL A: 256MB/512MB DDR3



18,20,22,34,43 +1.5V_VGA +1.5V_VGA

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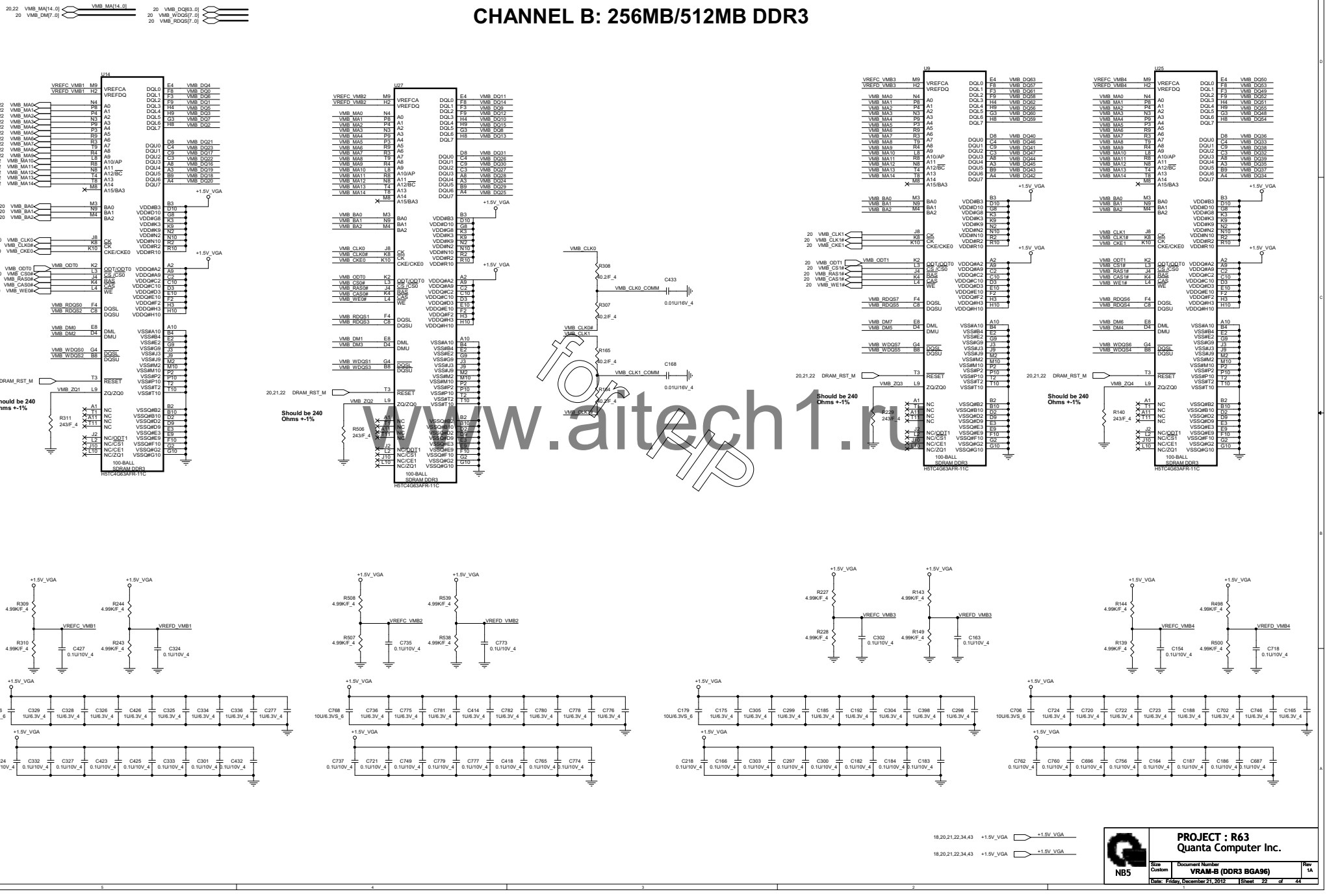
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	VRAM-A (DDR3 BGA96)	3A

Date: Friday, December 21, 2012 Sheet 21 of 44

CHANNEL B: 256MB/512MB DDR3

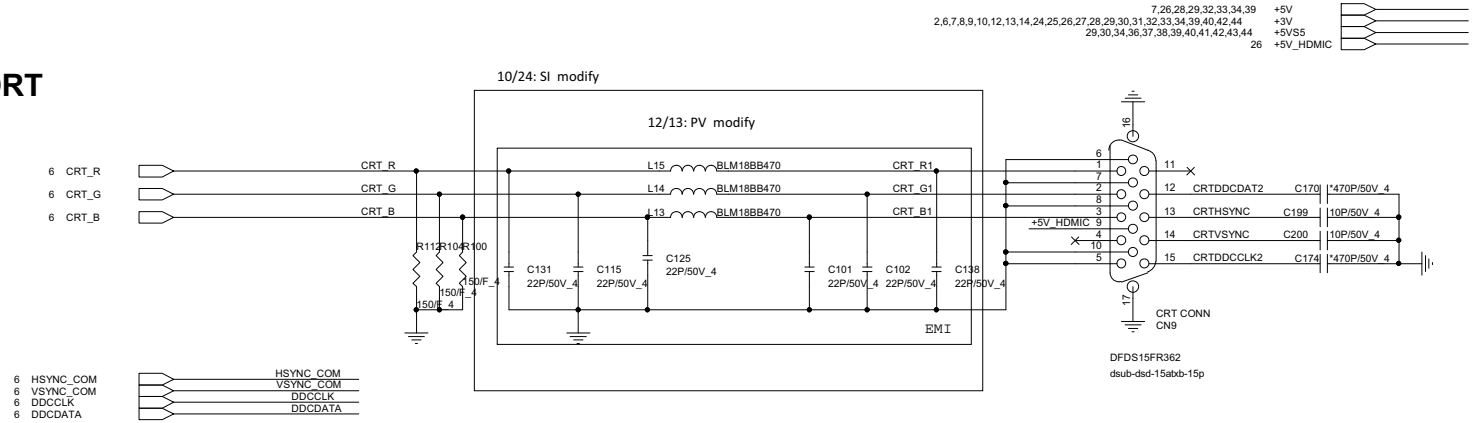


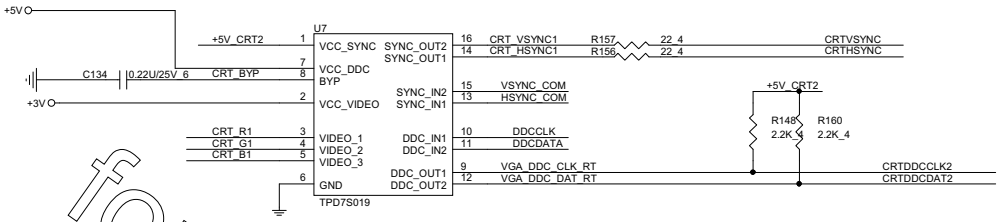
18,20,21,22,34,43 +1.5V_VGA → +1.5V_VGA

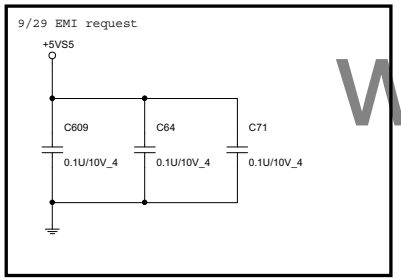
18,20,21,22,34,43 +1.5V_VGA → +1.5V_VGA

PROJECT : R63	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: VRAM-B (DDR3 BGA96); Rev: 1A
Date: Friday, December 21, 2012	Sheet 22 of 44

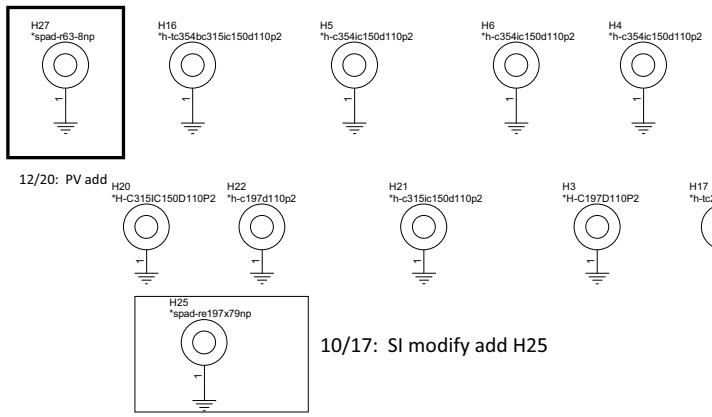
CRT PORT

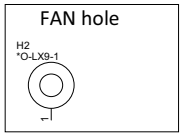


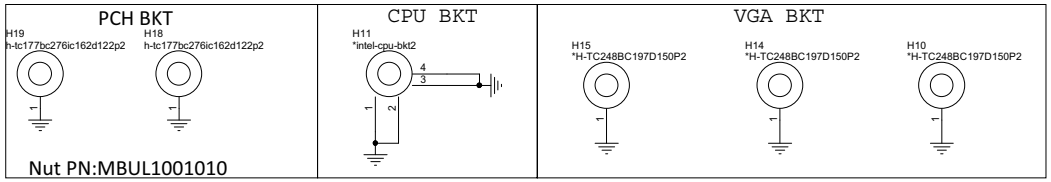


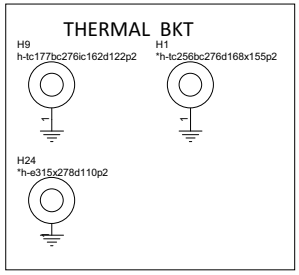


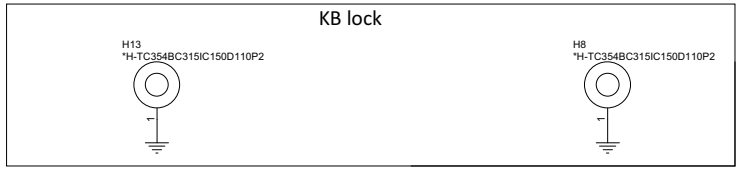
HOLE











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NB5

Size	Document Number	Rev
Custom	CRT,Hole	1A

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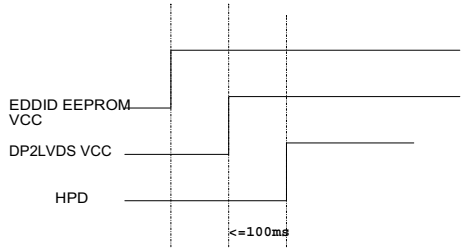
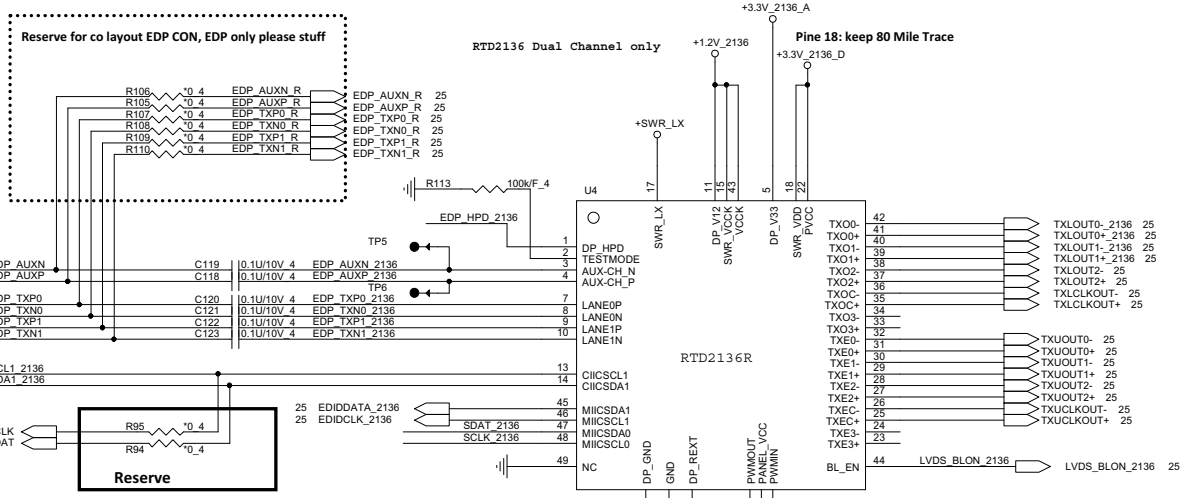
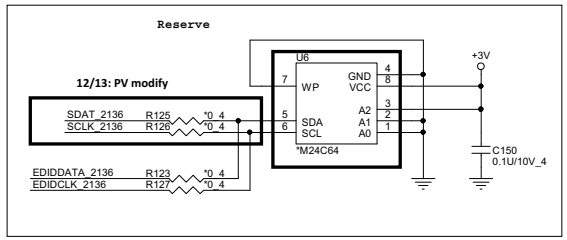
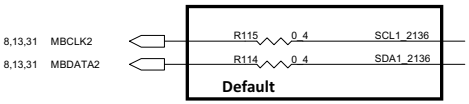
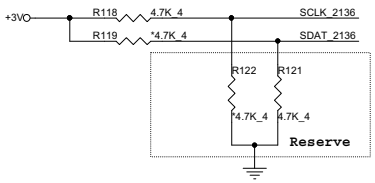
RTD2136S Power Up Sequence 24

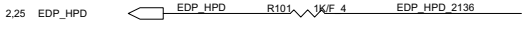






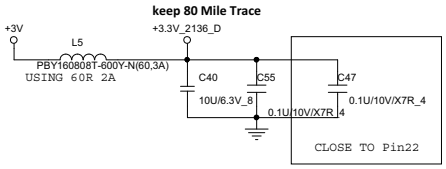


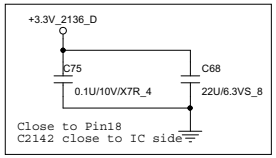


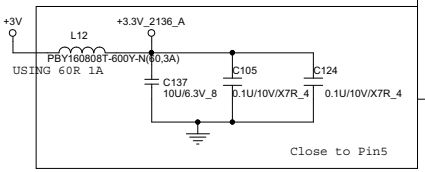


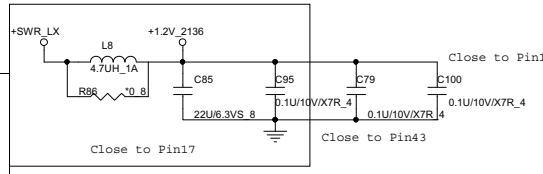
2,6,7,8,9,10,12,13,14,23,25,26,27,28,29,30,31,32,33,34,39,40,42,44 +3V

L8: need use CV-4709MN00 for Vendor suggestion









SWR MODE	LDO MODE
Stuff L8	Stuff R86

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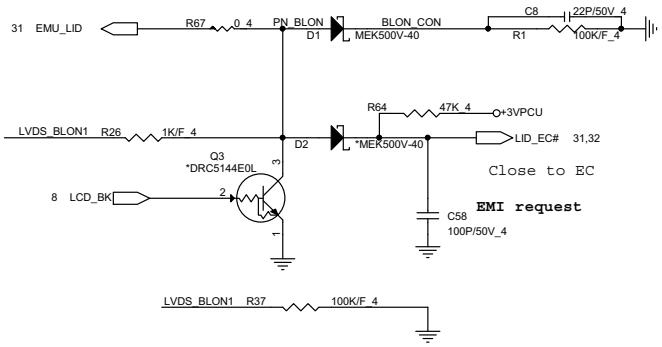
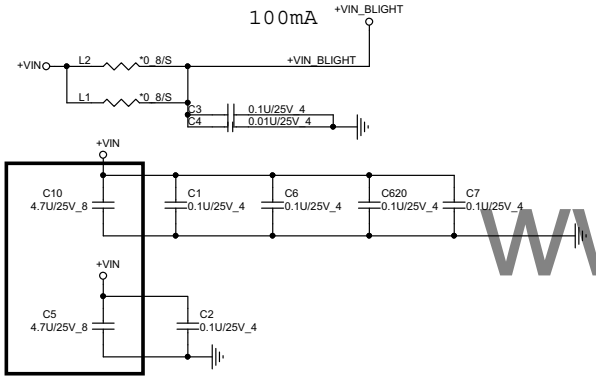
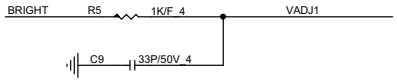
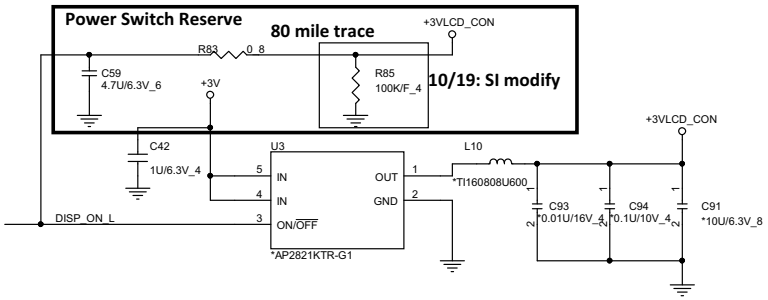
LID Switch

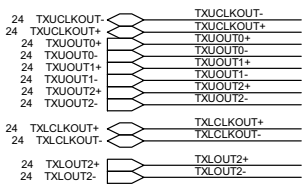


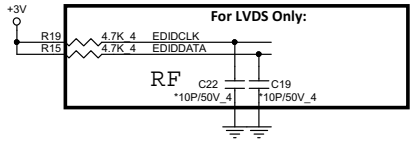


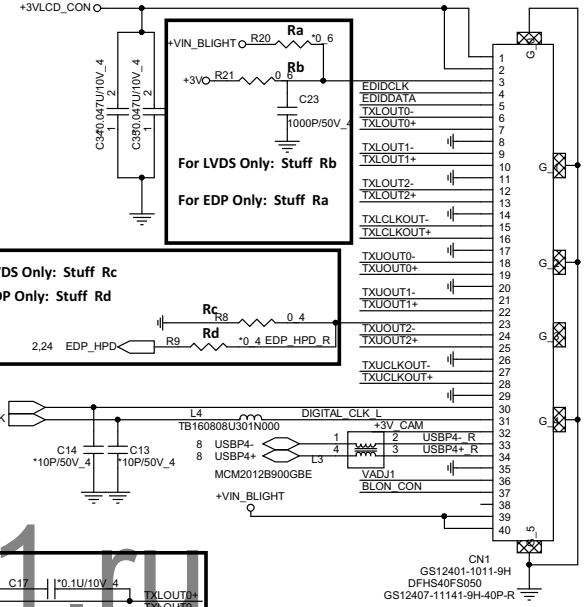
12/17: PV modify pn for 0.85 height

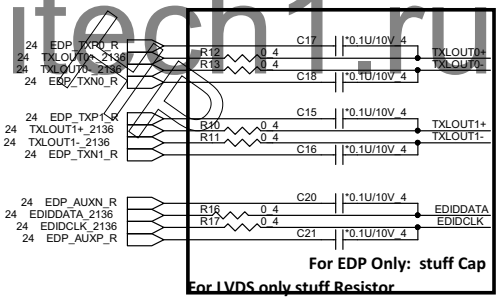


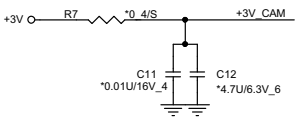


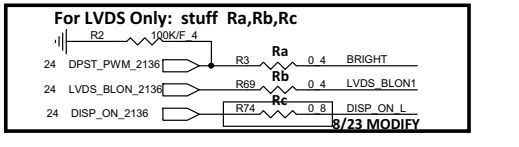


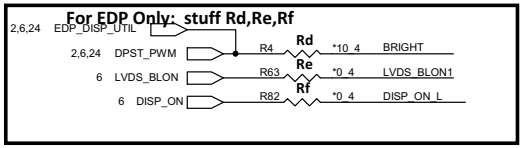


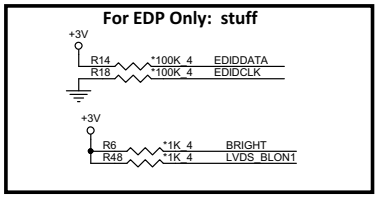


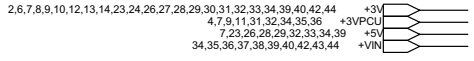












NB5

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Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
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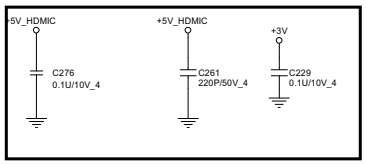
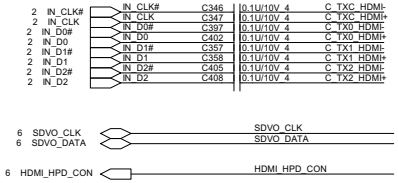
7,23,28,29,32,33,34,39 +5V
23 +5V_HDMIC
2,6,7,8,9,10,12,13,14,23,24,25,27,28,29,30,31,32,33,34,39,40,42,44 +3V

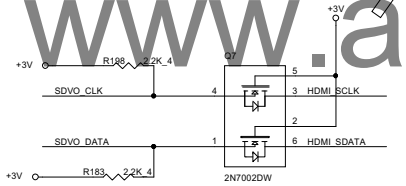
EMI request



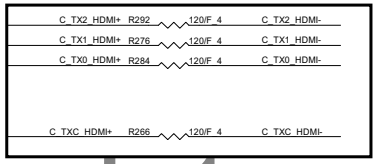
close to HDMI conn

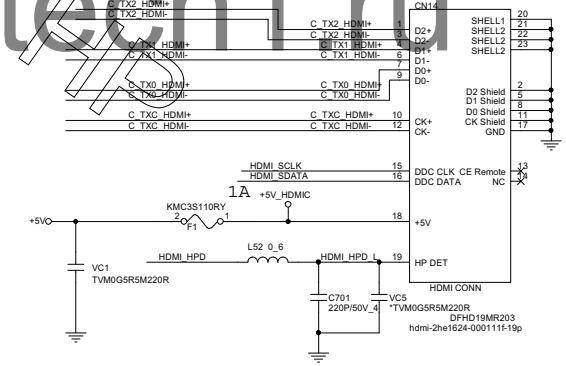


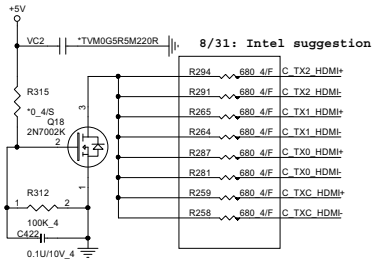
Close to HDMI Connector

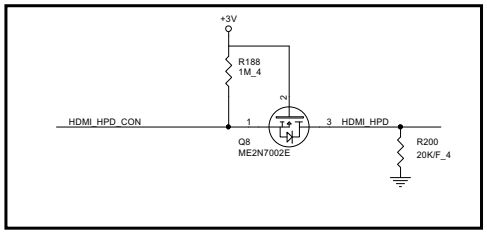


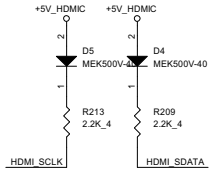
10/14: SI for EMI request







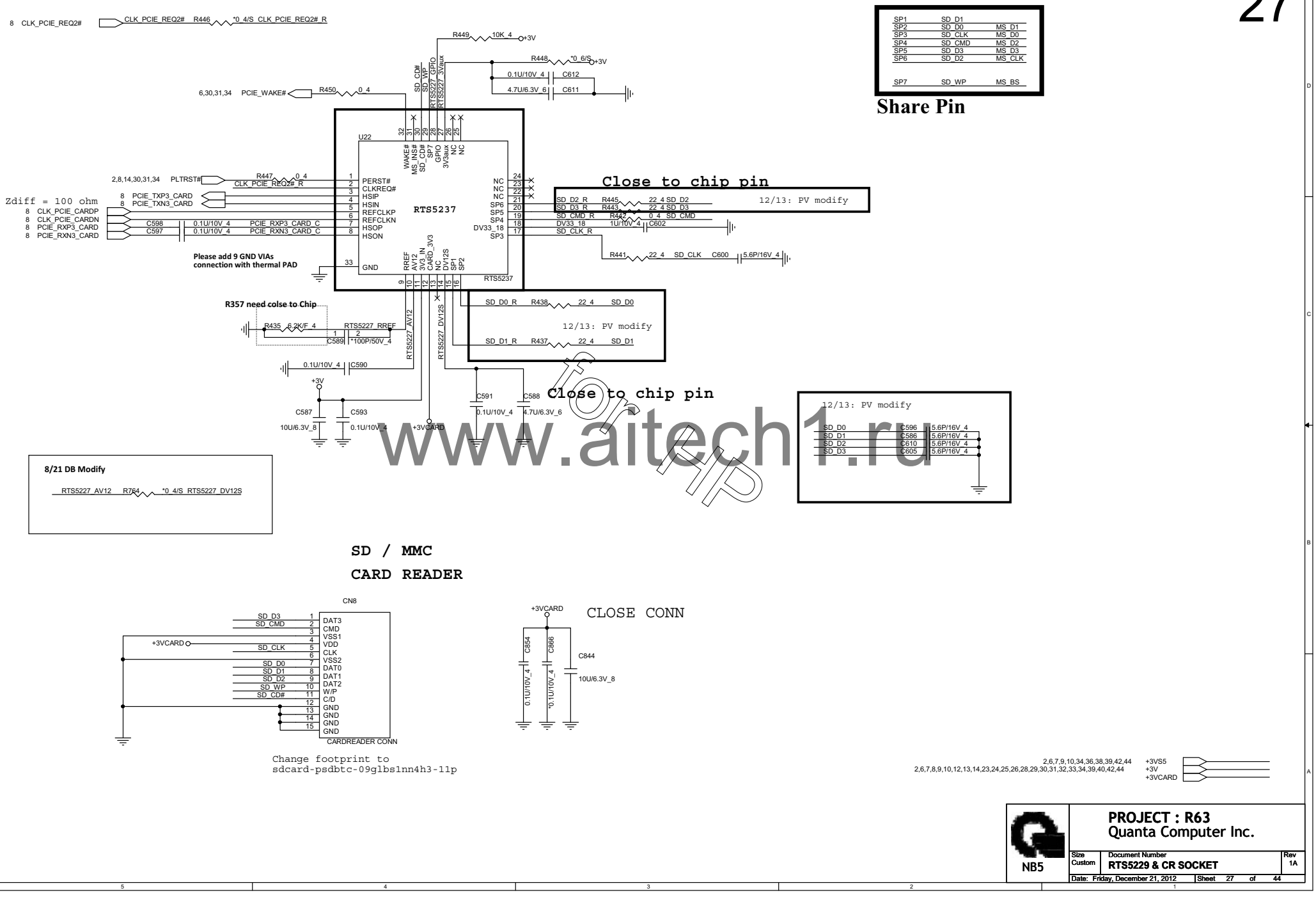




NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	1A
Date: Friday, December 21, 2012	Sheet 26 of 44	

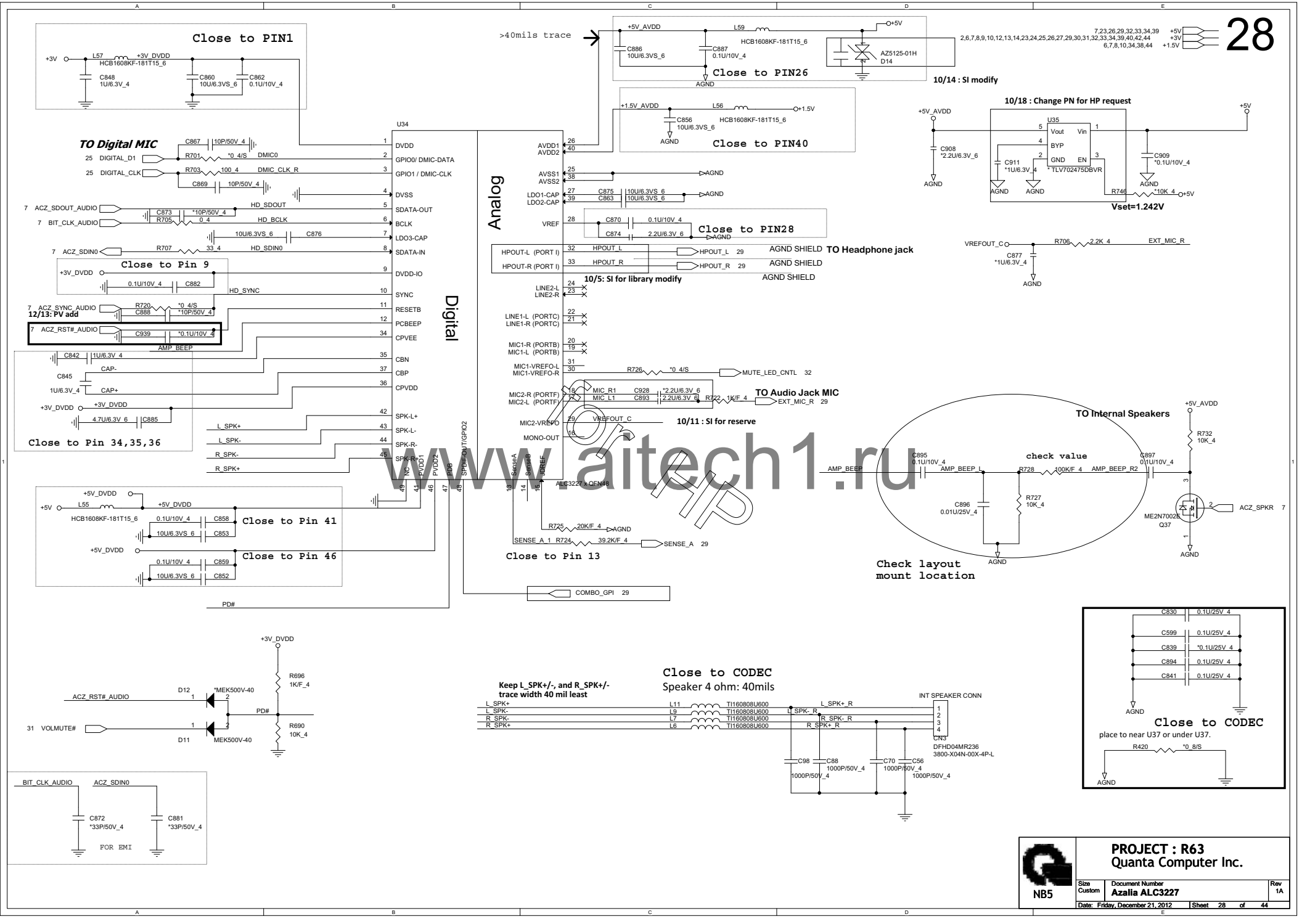


SD / MMC
CARD READER

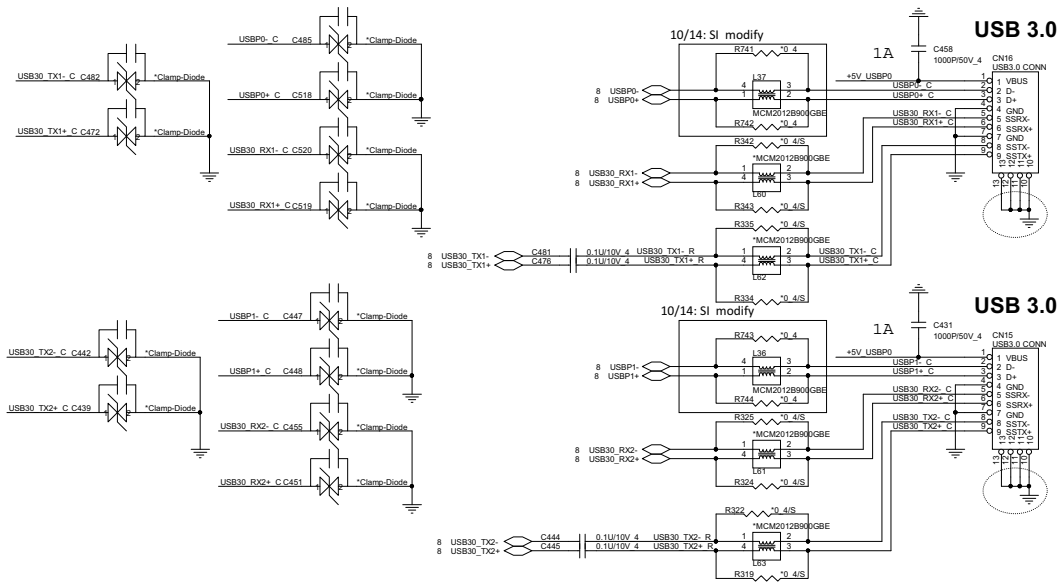
Change footprint to
sdcard-psdbtc-09glbs1nn4h3-11p

2,6,7,9,10,34,36,38,39,42,44 +3VS5
2,6,7,8,9,10,12,13,14,23,24,25,26,28,29,30,31,32,33,34,39,40,42,44 +3V
+3VCARD

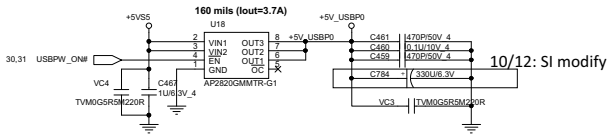
NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: RTS5229 & CR SOCKET	Rev: 1A
Date: Friday, December 21, 2012	Sheet 27 of 44	



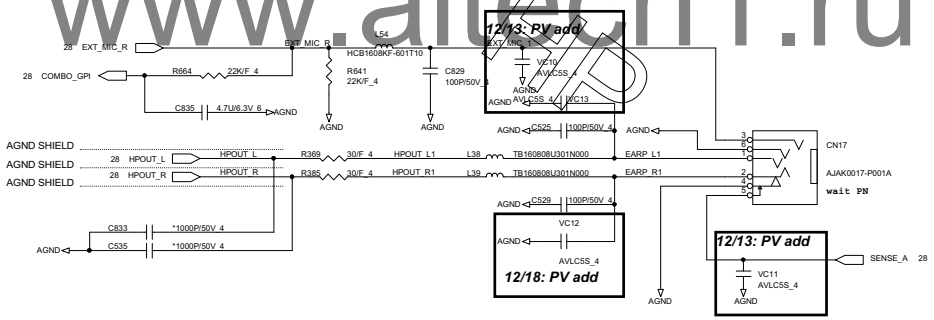
NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: Azalia ALC3227	Rev: 1A
Date: Friday, December 21, 2012	Sheet 28 of 44	



USB3.0 X 2/USB2.0 COMBO

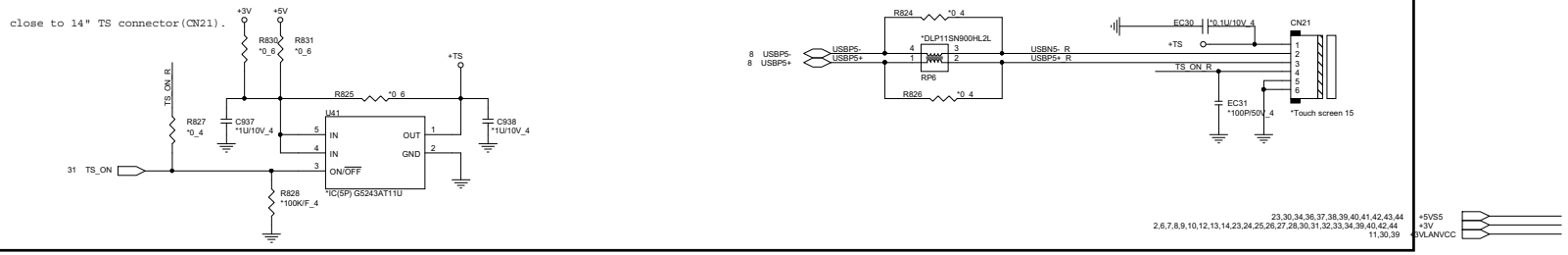


COMBO JACK



12/11: PV add

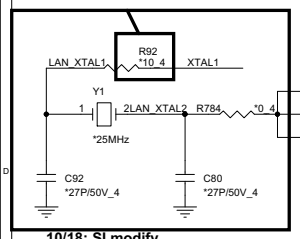
Touch Screen Connector



23,30,34,36,37,38,39,40,41,42,43,44 +5VS5
2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,30,31,32,33,34,39,40,42,44 +3V
11,30,39 +3VLANVCC

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: USB/BT/Audio JacK	Rev: 1A
Date: Friday, December 21, 2012	Sheet 29 of 44	

For EMI 0 ~ 22 ohm



10/18: SI modify

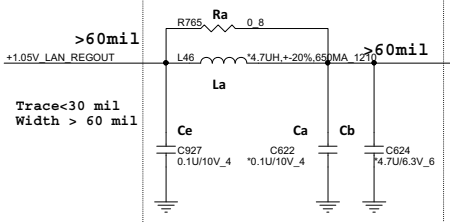
Green Clk

R53 0_4 LAN_XTAL25_IN 11

R89 *22_4 CLK_FLEX1_48M 8

XTAL2

Power trace Layout 寬度> 60mil

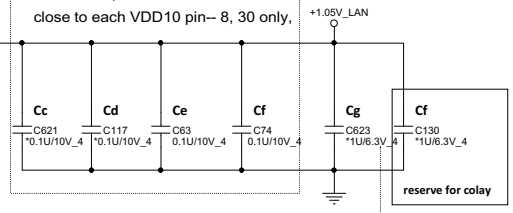


For GbE
Stuff La, Ca ,Cb

For 10/100
NA: La, Ca ,Cb
STUFF : Ra, Ce

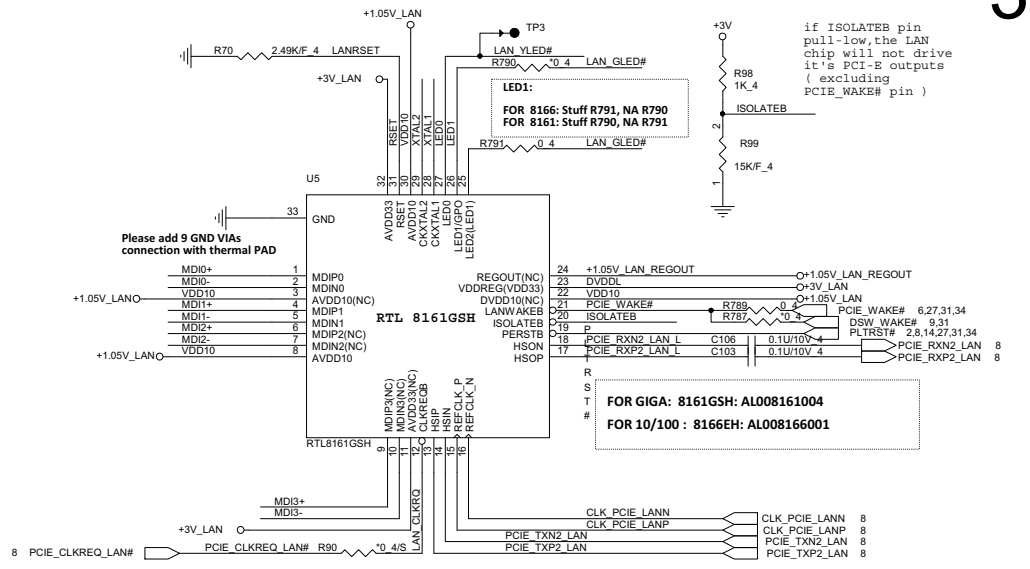
For GbE
* Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3, 22, 8 , 30

For 10/100 NA Ce,Cf
* Place Ce , Cf
close to each VDD10 pin-- 8, 30 only,



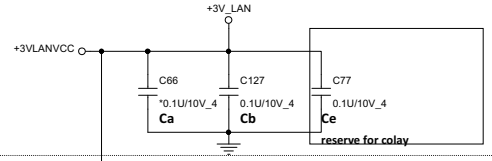
For GbE
* Place Cf close to each VDD10 pin-- 22 (reserve)

For 10/100
* Place Cg close to each VDD10 pin-- 30 (reserve)

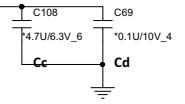


For 10/100
* Stuff Cb and Ce only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



* Place Cc and Cd close to each VDD33 pin-- 23

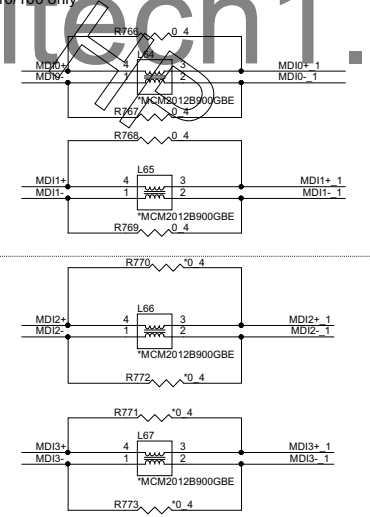


For GIGA
Stuff Cc ,Cd

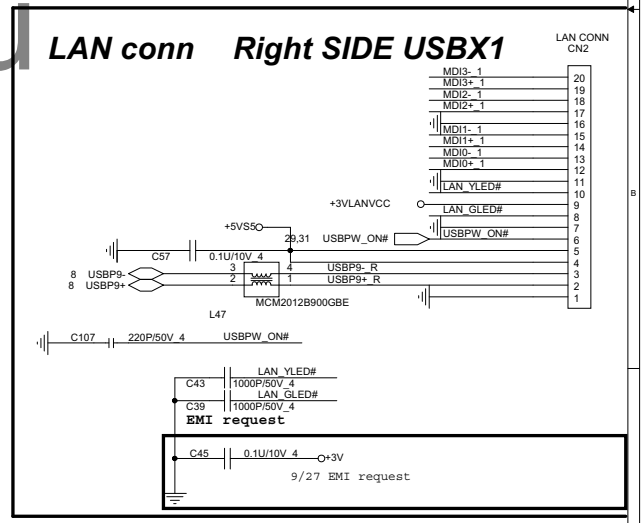
For 10/100
NA: Cc, Cd

Remove For Not Using SWR mode

For 10/100 only



LAN conn Right SIDE USBX1



For GiGA

BOT:GST5009B LF,DB0Z06LAN00

FCE :NS892407 ,DB0LL1LAN00

For 10/100

BOT: TST1284R LF DB0EL5LAN00

FCE :NS892408 ,DB0EF7LAN01

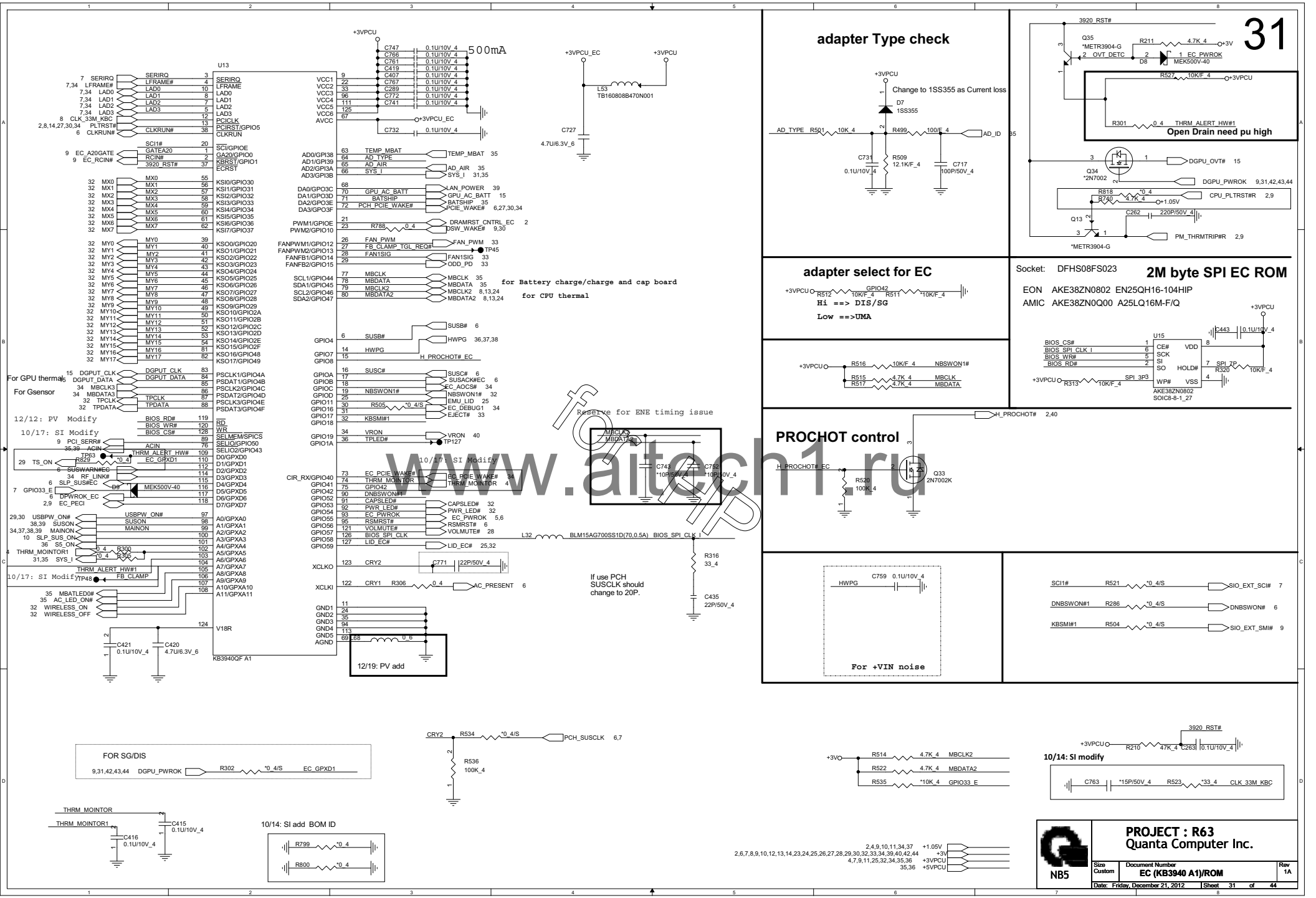
2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,31,32,33,34,39,40,42,44 +3V
11,39 +3VLANVCC

NB5

PROJECT : R63
Quanta Computer Inc.

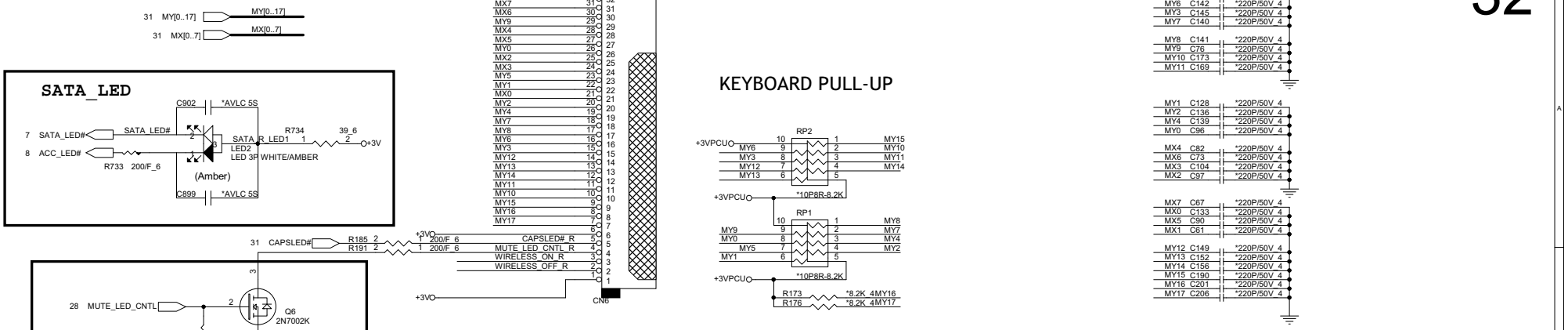
Size	Document Number	Rev
Custom	RTL 8105E/RJ45	1A

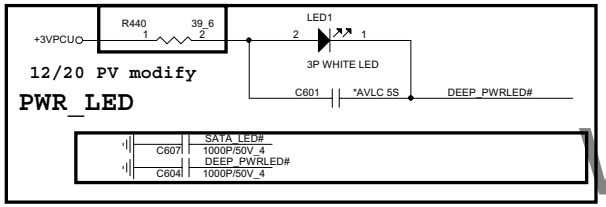
Date: Friday, December 21, 2012 Sheet 30 of 44

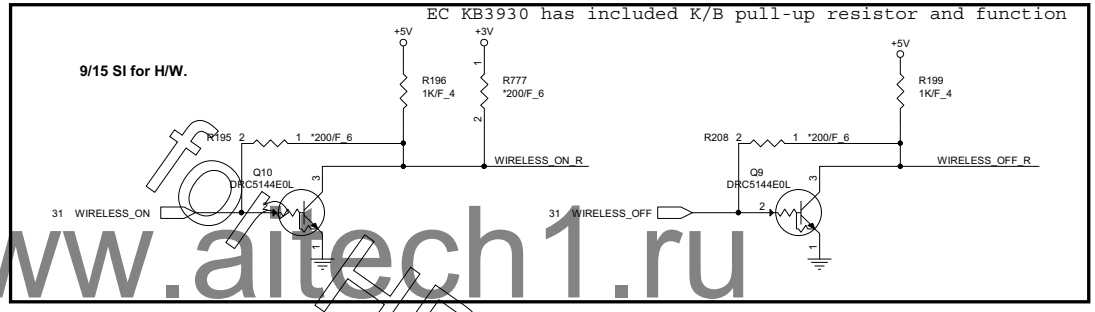


PROJECT : R63	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: EC (KB3940 A1)/ROM
Rev: 1A	
Date: Friday, December 21, 2012	Sheet 31 of 44

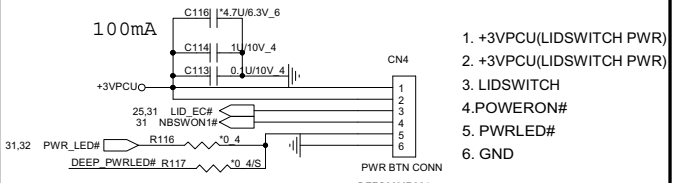
KEYBOARD Con.

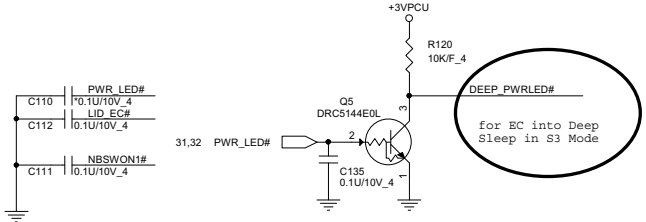




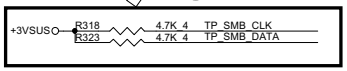


POWER BOTTON CONNECT

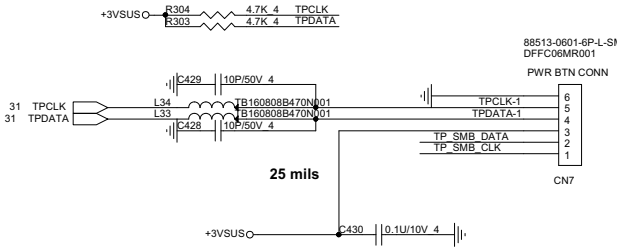


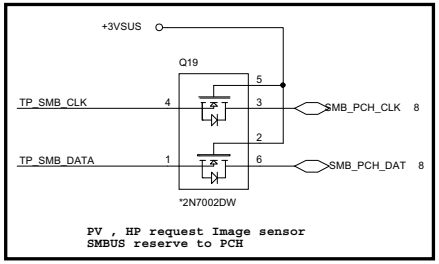


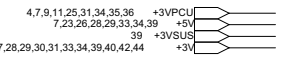
TOUCH PAD Con.



change to +3VSUS
close conn

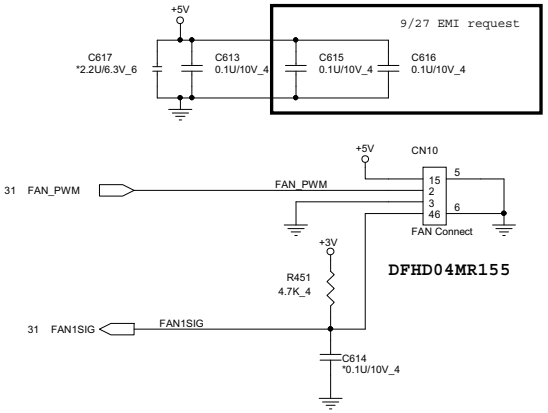






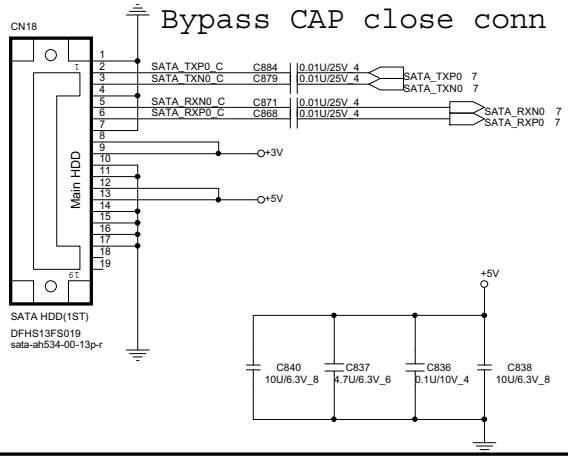
NB5	PROJECT : R63 Quanta Computer Inc.
Size: Custom	Document Number: LED/KB/SW/TP
Rev: 1A	
Date: Friday, December 21, 2012	Sheet 32 of 44

CPU FAN

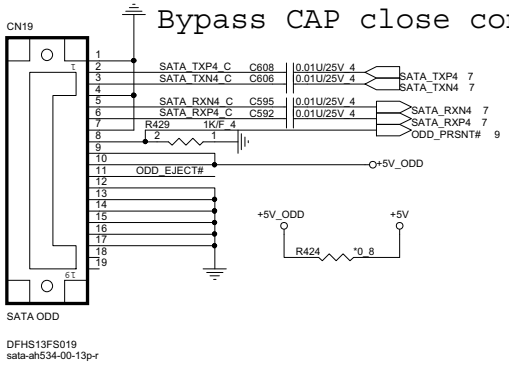


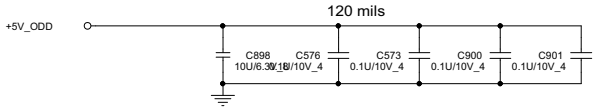
DFHD04MR155

SATA HDD CONNECTOR

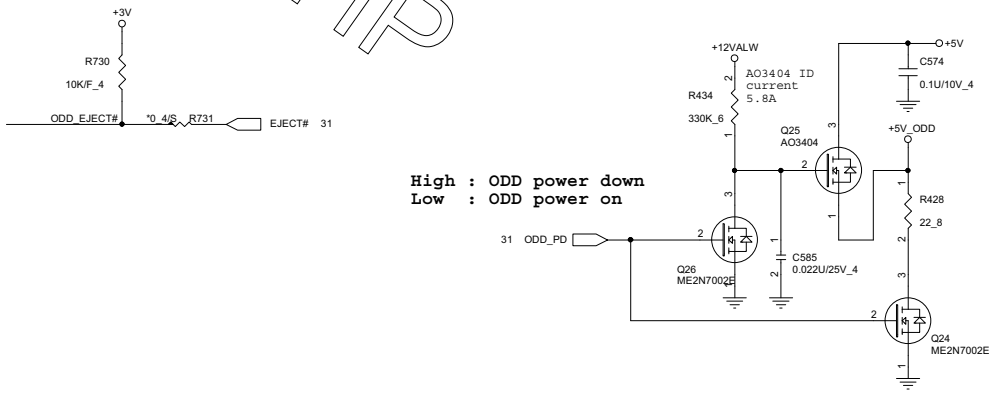


SATA ODD CONNECTOR





follow INTEL DG change eject PU to +3V.



High : ODD power down
Low : ODD power on

2,6,7,8,9,10,12,13,14,23,24,25,26,27,28,29,30,31,32,34,39,40,42,44 +3V
4,7,9,11,25,31,32,34,35,36 +3VPCU
7,23,26,28,29,32,34,39 +5V
35,39,44 +12VALW

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

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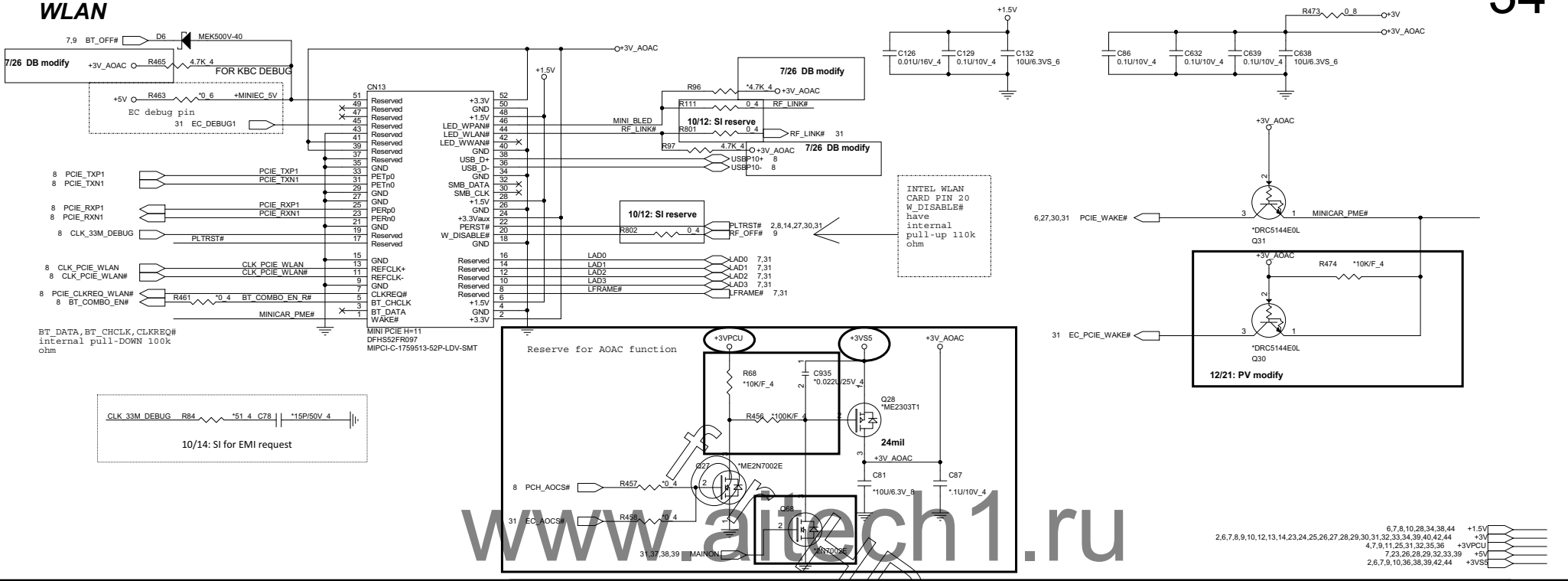
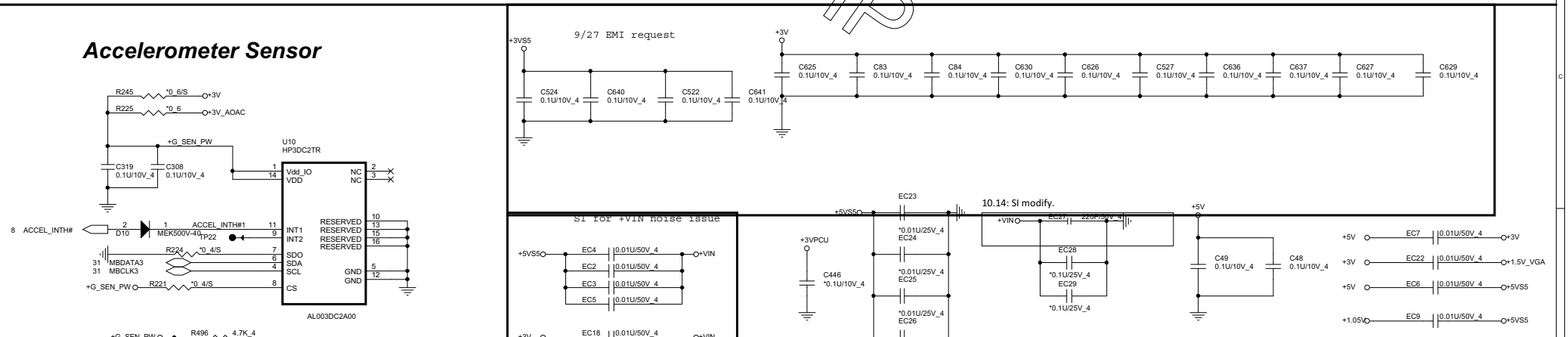
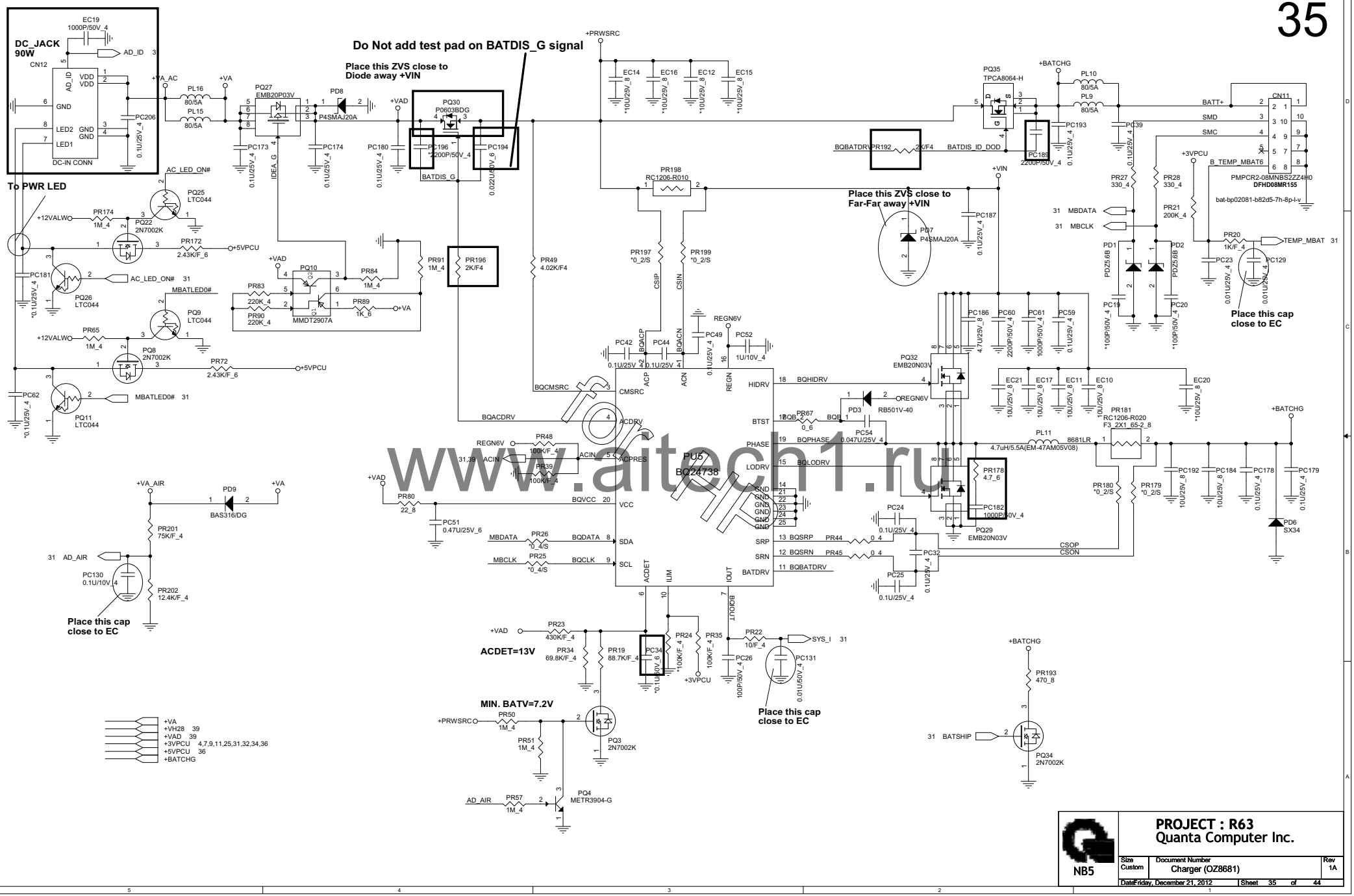
Mini PCI-E Card 1
WLAN



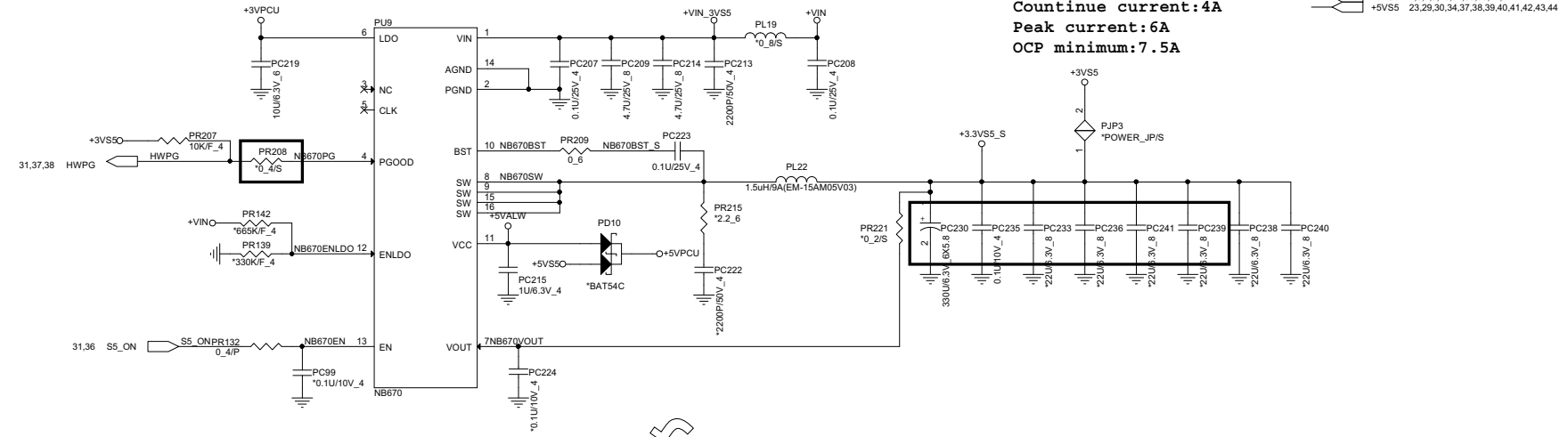


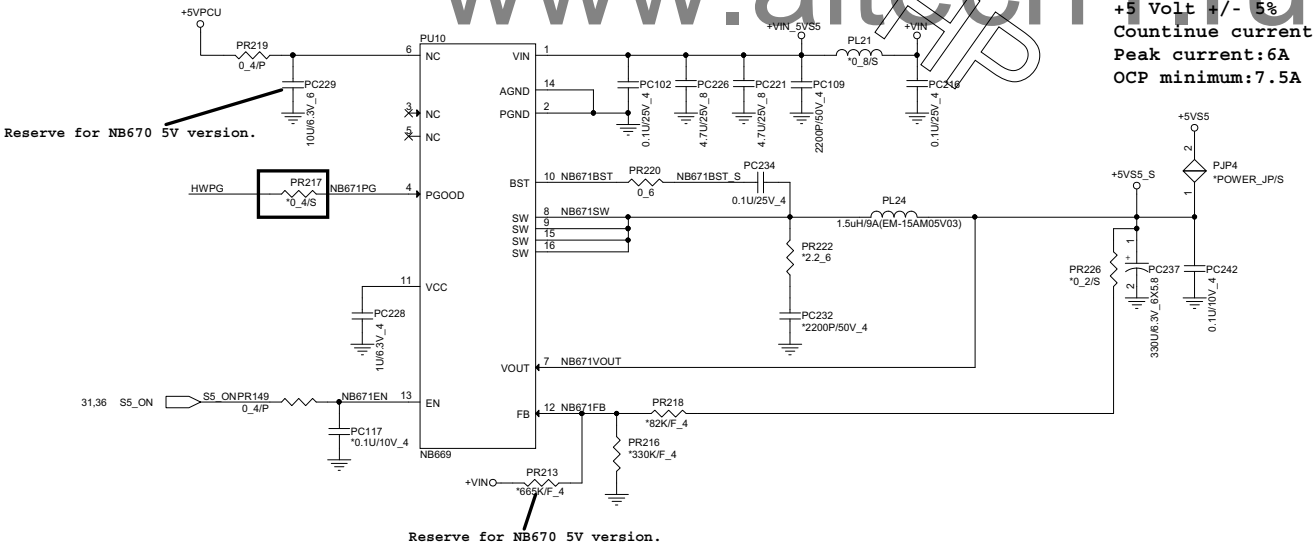
PROJECT : R63 Quanta Computer Inc.			
NB5	Size: Custom	Document Number: MINI PCIE CONN & G-sensor	Rev: 1A
	Date: Friday, December 21, 2012	Sheet 34 of 44	

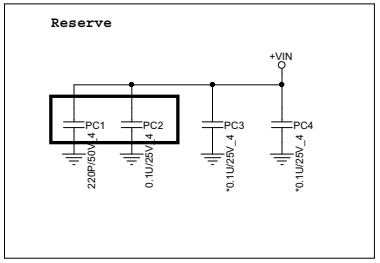


+VA	
+VH28	39
+VAD	39
+3VPCU	4,7,9,11,25,31,32,34,36
+5VPCU	36
+BATCHG	

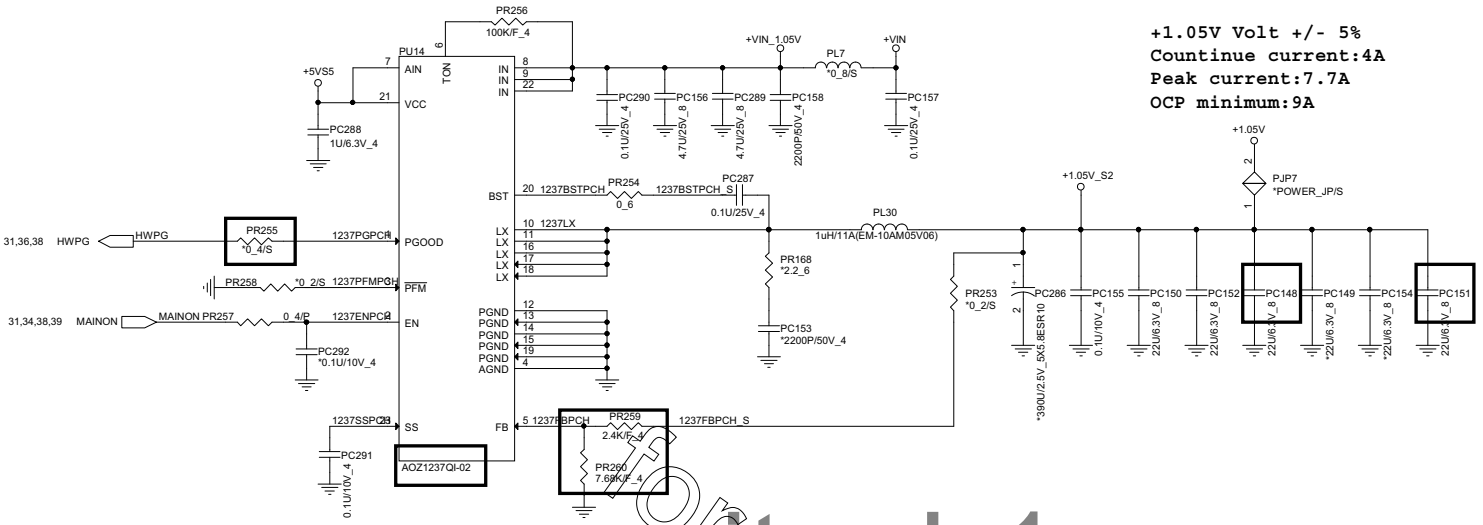
NB5	PROJECT : R63 Quanta Computer Inc.		
	Size: Custom	Document Number: Charger (OZ8681)	Rev: 1A
	Date: Friday, December 21, 2012	Sheet 35 of 44	







PROJECT : R63 Quanta Computer Inc.		
NB5	Size: Custom; Document Number: 3/5VPCU(RT8243A)	Rev: 1A
	Date: Friday, December 21, 2012	Sheet 36 of 44



+1.05V 2,4,9,10,11,31,34

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: 1.05V(RT8228BZ)	Rev: 1A
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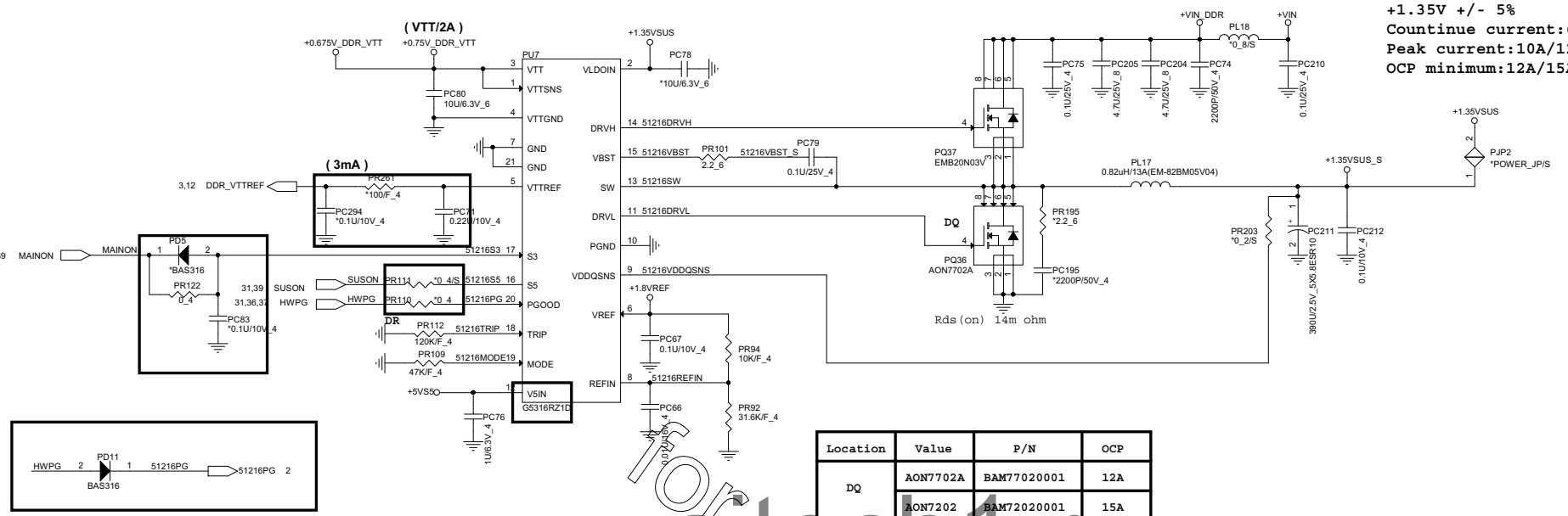
+1.35VSUS 2,3,4,12,13
+1.5V 6,7,8,10,28,34,44

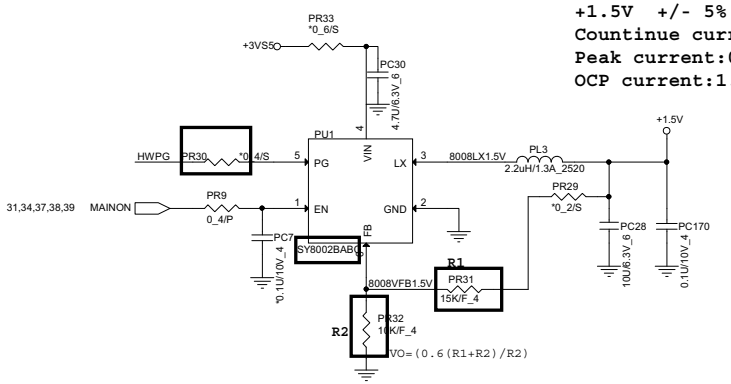
+1.35V +/- 5%
Countinue current:6A/8A
Peak current:10A/12A
OCP minimum:12A/15A



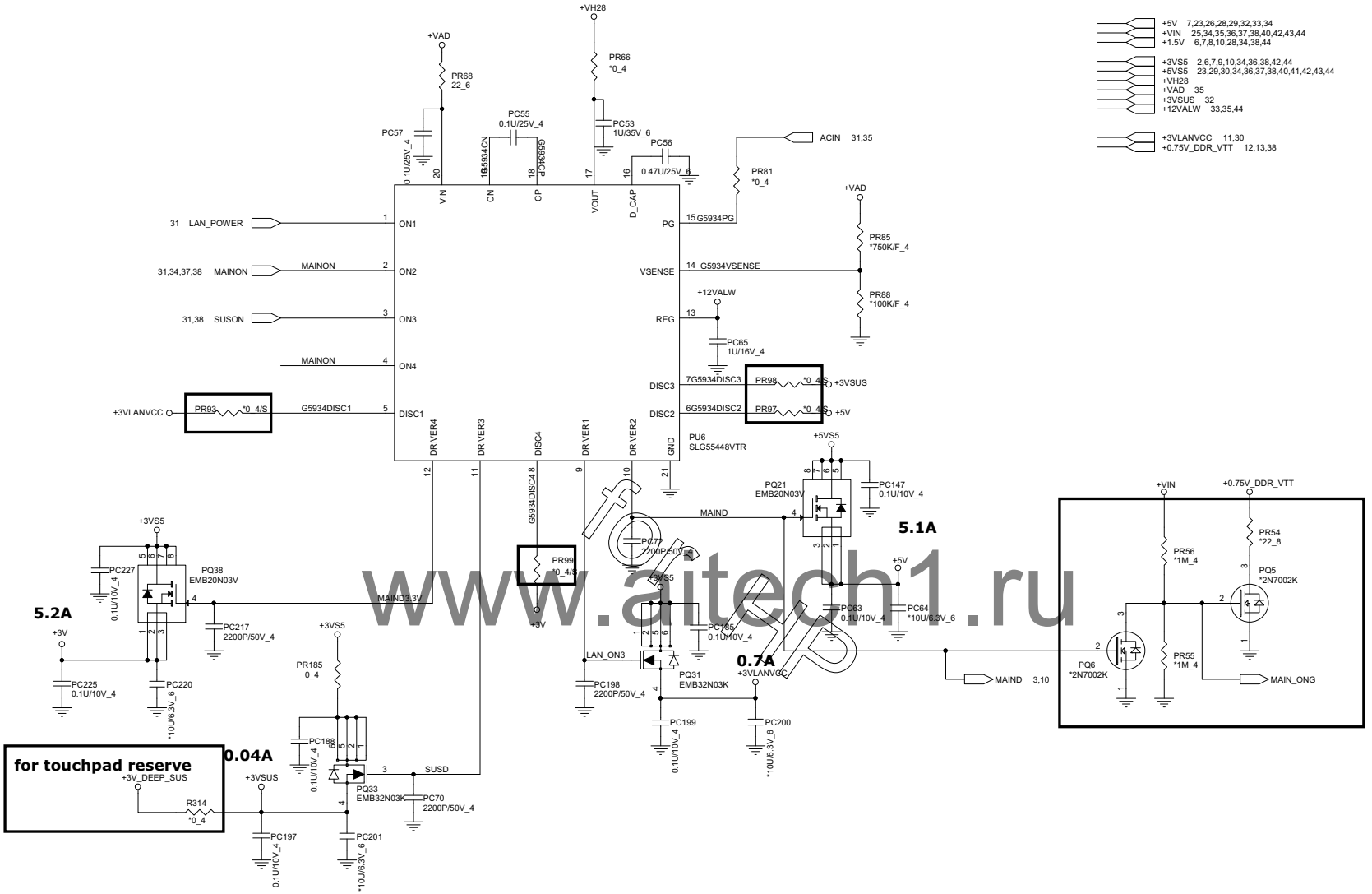
Location	Value	P/N	OCP
DQ	AON7702A	BAM77020001	12A
	AON7202	BAM72020001	15A

Location	Value	P/N	OCP
DR	120K	CS41202FB17	12A
	76.8K	CS37682FB00	15A

+1.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A
OCP current:1.2A



NB5	PROJECT : R63 Quanta Computer Inc.		
Size: Custom	Document Number: DDR3L(APW8819)		Rev: 1A
Date: Friday, December 21, 2012	Sheet 38 of 44		



+5V 7,23,26,28,29,32,33,34
+VIN 25,34,35,36,37,38,40,42,43,44
+1.5V 6,7,8,10,28,34,38,44

+3VS5 2,6,7,9,10,34,36,38,42,44
+5VS5 23,29,30,34,36,37,38,40,41,42,43,44
+VH28
+VAD 35
+3VSUS 32
+12VALW 33,35,44

+3VLANVCC 11,30
+0.75V_DDR_VTT 12,13,38

NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: Dis-charge IC (G5934)	Rev: 1A
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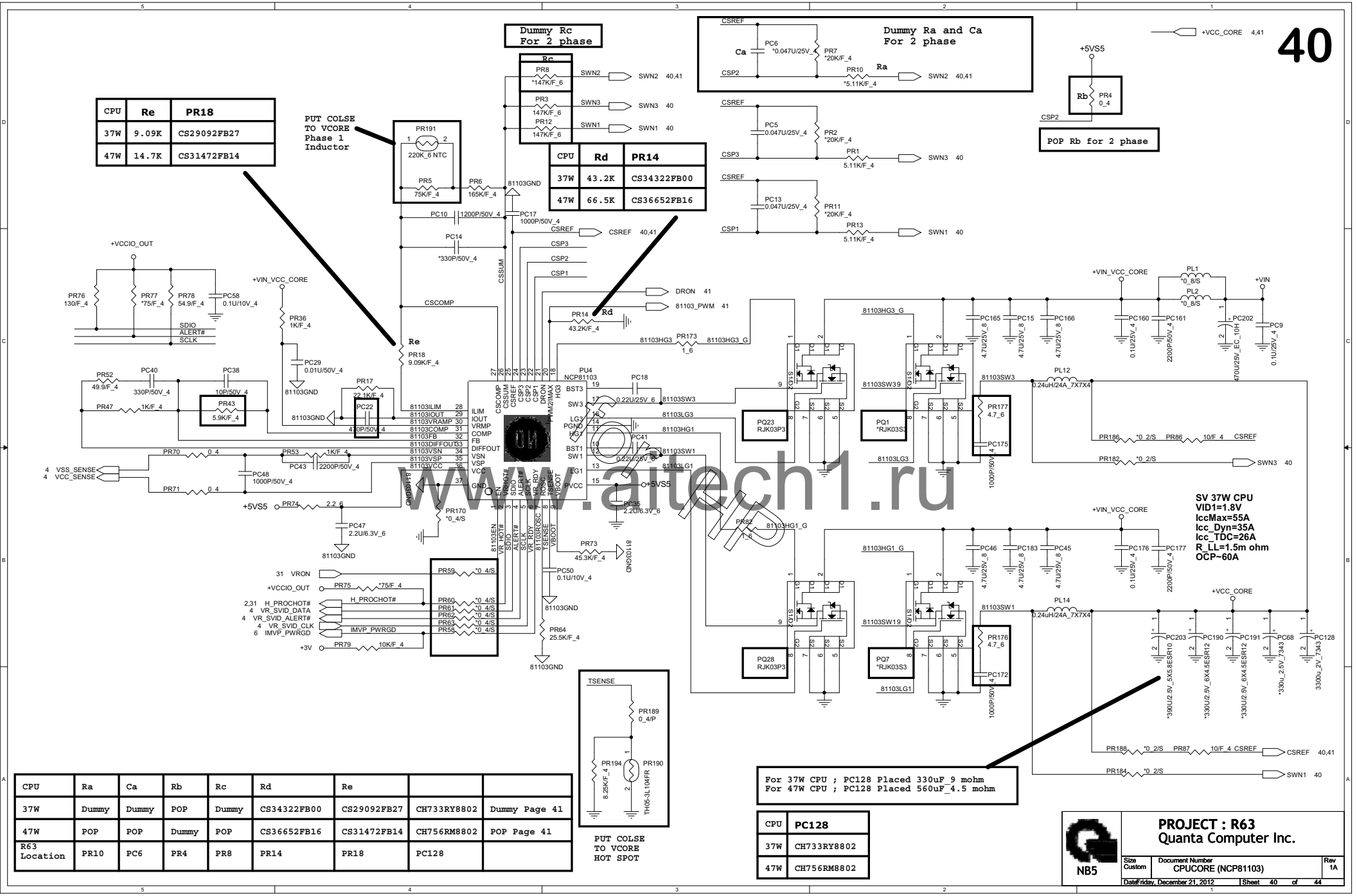

CPU	Re	PR18
37W	9.09K	CS29092FB27
47W	14.7K	CS31472FB14

CPU	Rd	PR14
37W	43.2K	CS34322FB00
47W	66.5K	CS36652FB16

CPU	PC128
37W	CH733RY8802
47W	CH756RM8802

CPU	Ra	Ca	Rb	Rc	Rd	Re		
37W	Dummy	Dummy	POP	Dummy	CS34322FB00	CS29092FB27	CH733RY8802	Dummy Page 41
47W	POP	POP	Dummy	POP	CS36652FB16	CS31472FB14	CH756RM8802	POP Page 41
R63 Location	PR10	PC6	PR4	PR8	PR14	PR18	PC128	

PROJECT : R63
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	CPUCORE (NCP81103)	1A

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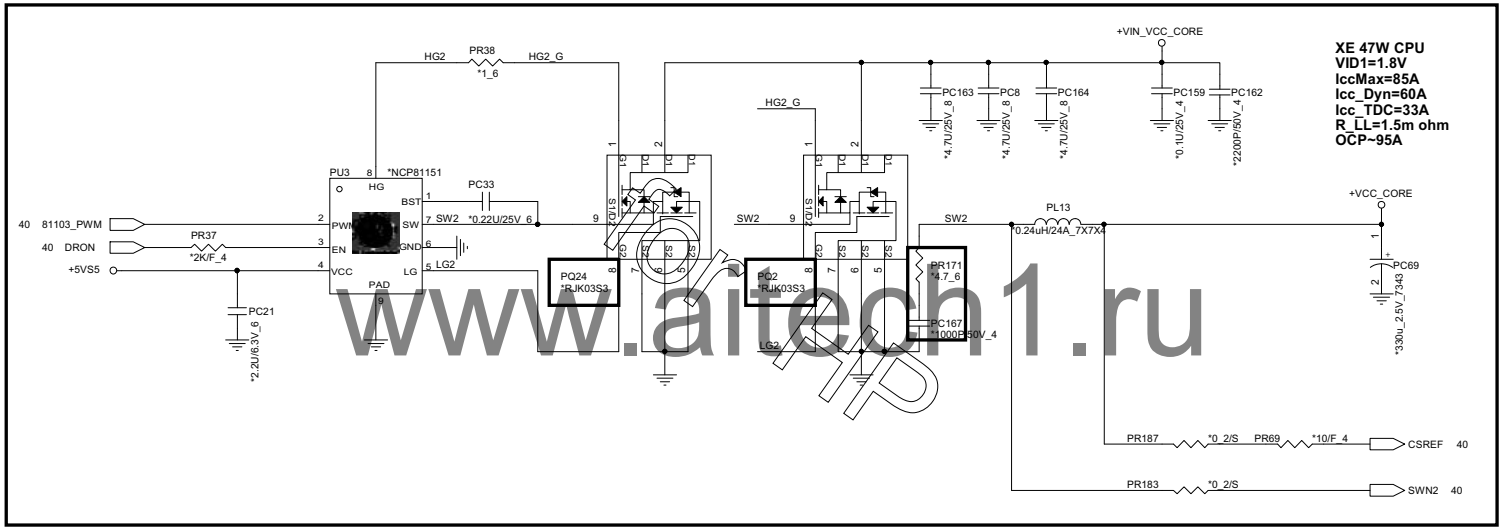

For 37W CPU
Dummy these components

+VCC_CORE 4,40

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NCP81151	1A

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VGA Core

+VGA_CORE 18,34,44

GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

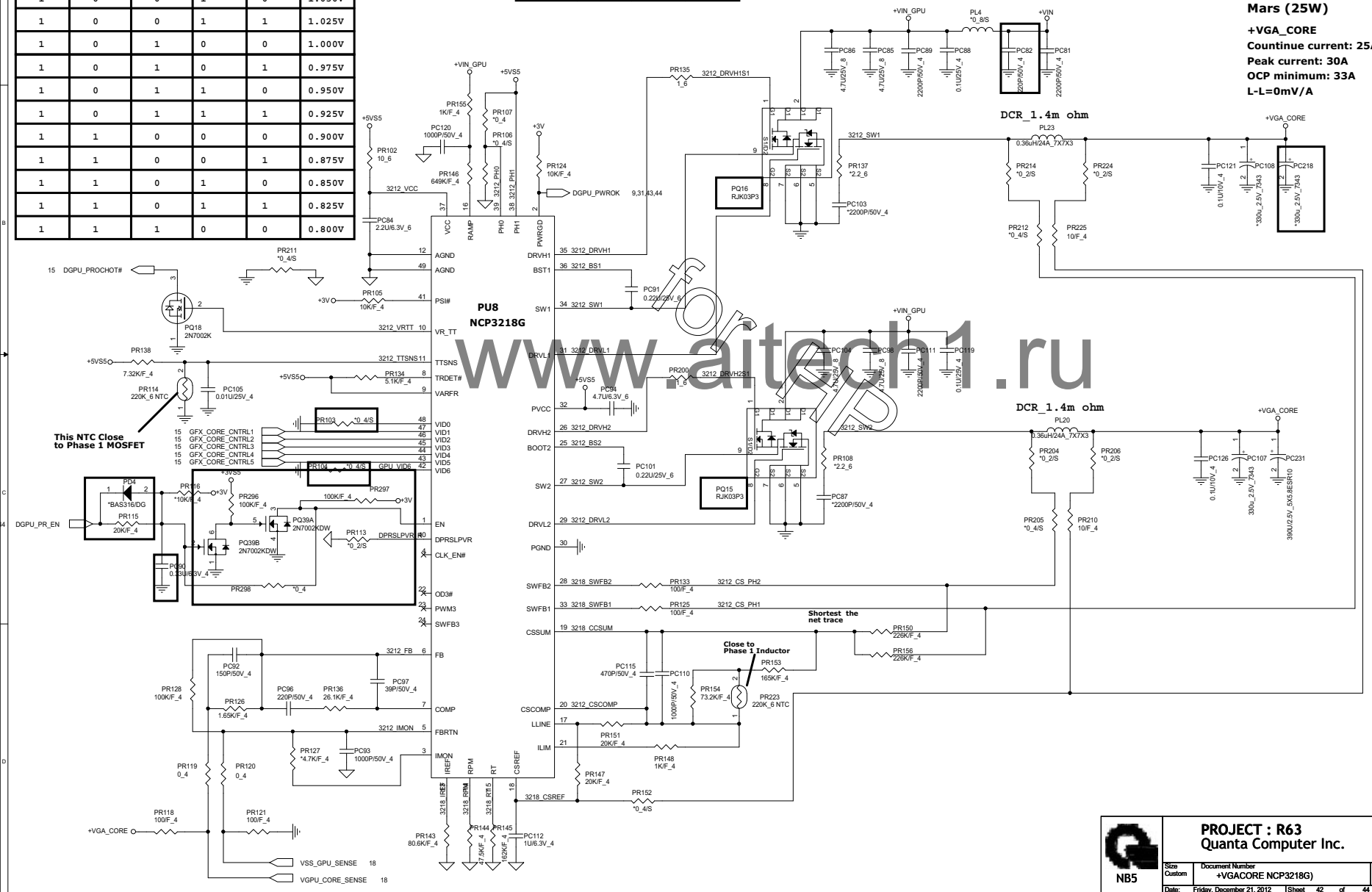
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE	
0	1	1	1	1	1.125V	
1	0	0	0	0	1.100V	Default
1	0	0	0	1	1.075V	
1	0	0	1	0	1.050V	
1	0	0	1	1	1.025V	
1	0	1	0	0	1.000V	
1	0	1	0	1	0.975V	
1	0	1	1	0	0.950V	
1	0	1	1	1	0.925V	
1	1	0	0	0	0.900V	
1	1	0	0	1	0.875V	
1	1	0	1	0	0.850V	
1	1	0	1	1	0.825V	
1	1	1	0	0	0.800V	

GPIO12 GPIO16 GPIO15 Thames XT

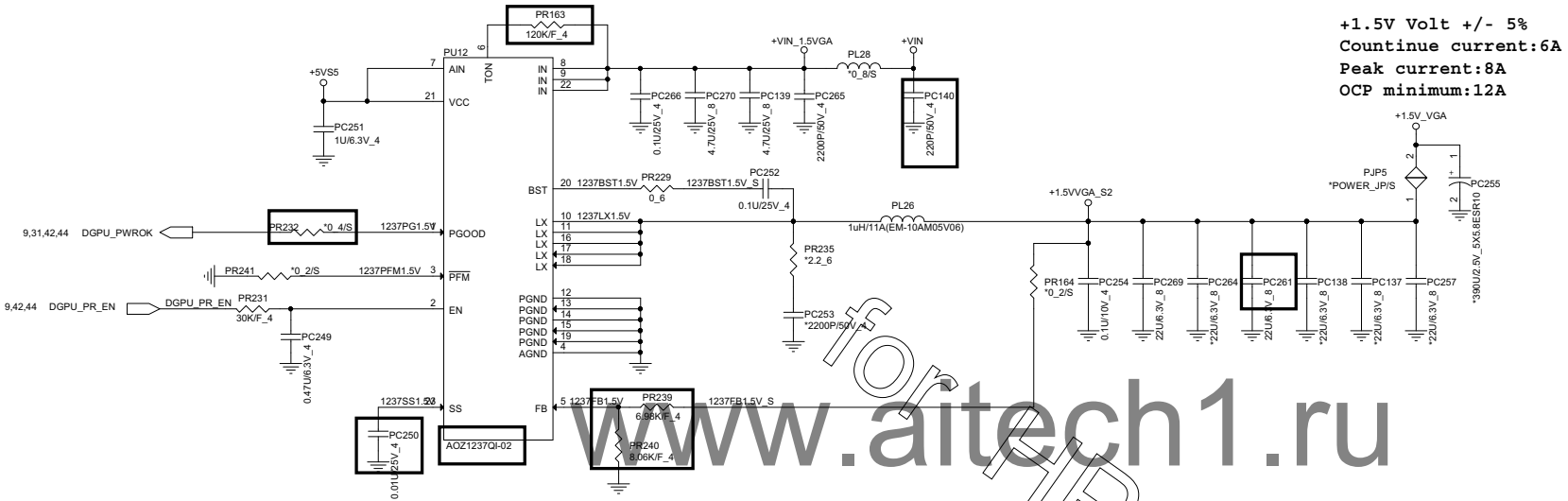
PWRCNTL4	PWRCNTL3	PWRCNTL1	V-CORE	
0	1	0	1.0V	Default
1	0	0	0.9V	
1	0	1	0.875V	

Mars (25W)

+VGA_CORE
Countinue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L=0mV/A



NB5	PROJECT : R63 Quanta Computer Inc.	
	Size: Custom Document Number: +VGACORE NCP3218G)	Rev: 1A
	Date: Friday, December 21, 2012 Sheet 42 of 44	



NB5	PROJECT : R63 Quanta Computer Inc.	
Size: Custom	Document Number: +VGA POWER	Rev: A
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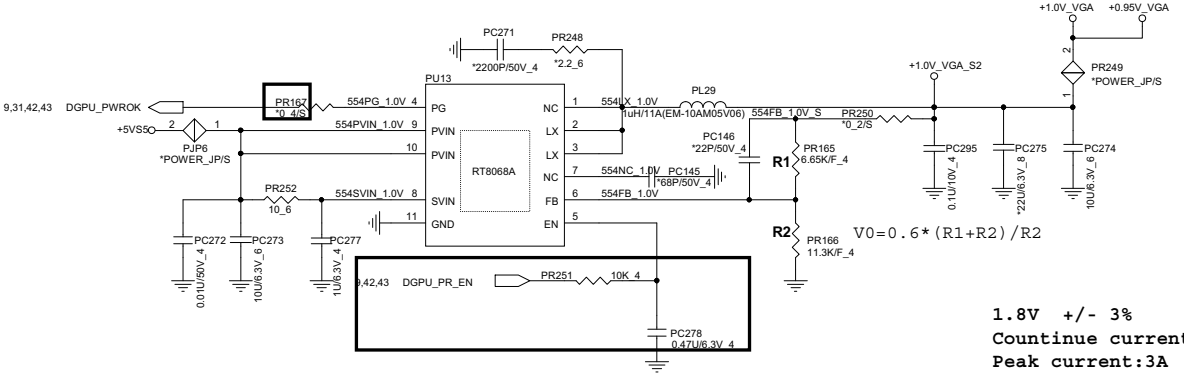
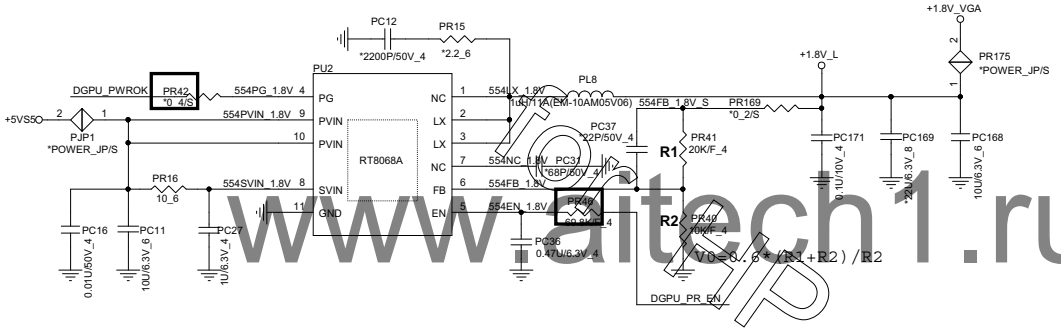
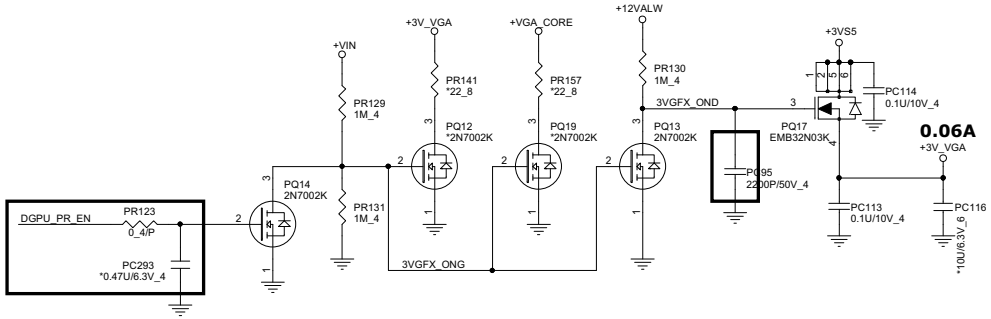
VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

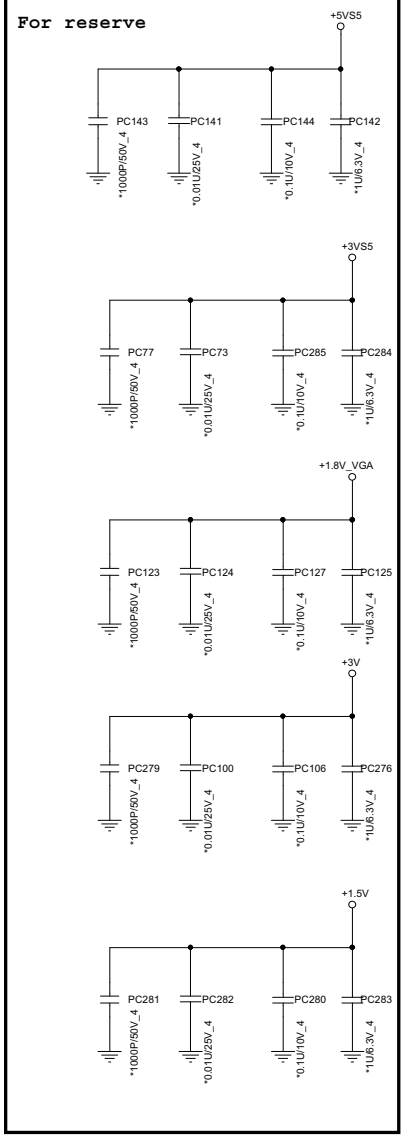


1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A





For reserve



+1.8V_VGA 11,15,16,18,19
+1.0V_VGA 14,16,18,19
+3V_VGA 14,18

NB5

PROJECT : R63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A
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